DESIGN CONSIDERATIONS

AM TRANSMITTERS

nautel

Making Digital Broadcasting Work.

Overview

- Design Criteria
- Modulation
- TX Block Diagram
- RF Amplifier
- Harmonic Filter
- Combiner
- Modulator
- Exciter
- Power Supply
- Circuit Board
- Cooling
- Protection

Design Criteria

Early conceptual design starts with knowing a desired RF output power and knowing the Regulatory Requirement governing the broadcast signal such as:

– CE RED

– FCC CFR47 Part 73

– Innovation, Science and Economic Development Canada BETS5

These regulations govern items such as occupied bandwidth, spurious and harmonic emissions, Audio quality, AM noise, FM noise, Electro-magnetic compatibility, safety.

Design Criteria

Other design considerations include:

- Reliability
- Redundancy
- Dollars per watt ($/W)
- Power density (W/in^3)
- Power conversion efficiency (operating cost)
- Feature set

These considerations can quite often conflict with each other such as redundancy and $/W.

Designers must understand and choose their guiding principals

Design Criteria

Nautel has always considered reliability one of the leading design principal and as such has an internal engineering document guiding our acceptable component stress.

Electrical stress, at its essence comes from two parameters:

– Voltage (Joules/coulomb) stress causing dielectric breakdown and dielectric heating

– Current (Coulombs/second) stress causing excessive heating of conductors ($P = i^2R$)

Design Criteria

Examples of Nautel design guidelines include:

– Resistors not to dissipate more than 50% of manufactures rating
– Capacitors operating voltage to be 66% of rating
– Voltage stress in air to be 5V/mil (breakdown at sea level occurs at 75V/mil in a uniform field)
– Transistor junction temperature not to exceed 75% of max rating under normal operating conditions

These guidelines have helped establish a history of highly reliable transmitters.

Design Criteria

Reliability and redundancy have also greatly influence Nautel designs. Going back to our roots, it was a request for improved MTBF that drove the first solid state designs as the Nav Canada needed ultra reliable transmitters in northern Canada which tube designs of the day could not meet.

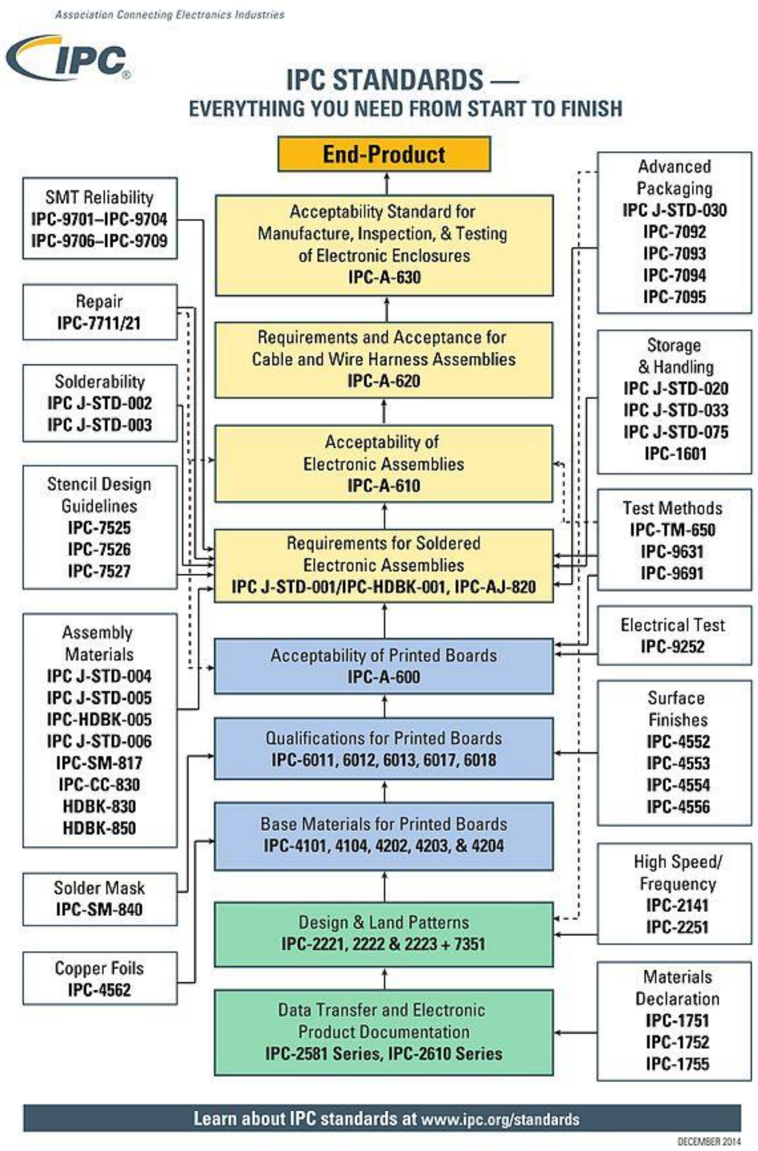
Design Criteria

We continue to build the majority of our design redundancy in mind including:

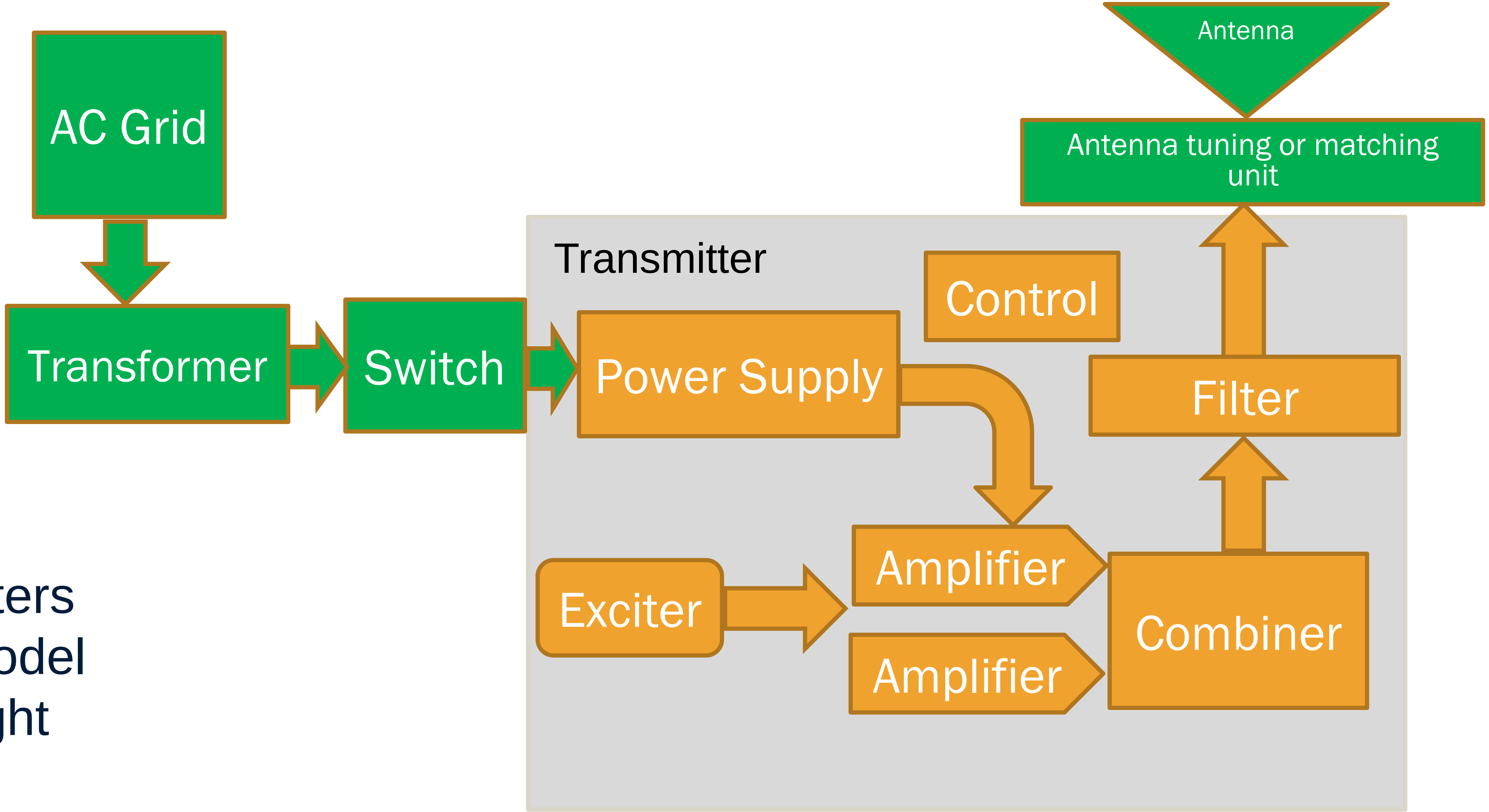
- multiple parallel amplifiers that can be hot serviced
- dual exciters
- dual low voltage power supplies
- Multiple parallel cooling fans

Design Criteria

Nautel also uses IPC standards to guide the construction of all electronic assemblies.



Generic Transmitter Block Diagram



Most transmitters fit the model to the right

Modulation Design

- Modulation techniques
  - Linear amplification
  - Single Pulse Duration Modulation (PDM)
  - Bi-Phase Pulse Duration Modulation (PDM)
  - Multi Phase Pulse Duration Modulation (PDM)
  - Pulse Step Modulation
  - Pulse Step Modulation with step interpolation

Modulation Design

$$e = (1 + M \sin \omega_m t) . \sin(\omega_c t)$$

Where

M is modulation index
$\sin \omega_m t$ is modulating frequency
$\sin(\omega_c t)$ is the carrier frequency

Modulation Design

Consider a carrier wave (sine wave) of frequency f_c and amplitude A given by:

$$c(t) = A \cdot \sin(2\pi f_c t)$$

Let $m(t)$ represent the modulation waveform. For this example, we shall take the modulation to be simply a sine wave of a frequency f_m, a much lower frequency (such as an audio frequency) than f_c:

$$m(t) = M \cdot \cos(2\pi f_m t + \phi)$$

where M is the amplitude of the modulation. We shall insist that $M<1$ so that $(1+m(t))$ is always positive. If $M>1$ then overmodulation occurs and reconstruction of message signal from the transmitted signal would lead in loss of original signal. Amplitude modulation results when the carrier $c(t)$ is multiplied by the positive quantity $(1+m(t))$:

$$y(t) = [1 + m(t)] \cdot c(t)$$

$$= [1 + M \cdot \cos(2\pi f_m t + \phi)] \cdot A \cdot \sin(2\pi f_c t)$$

Modulation Design

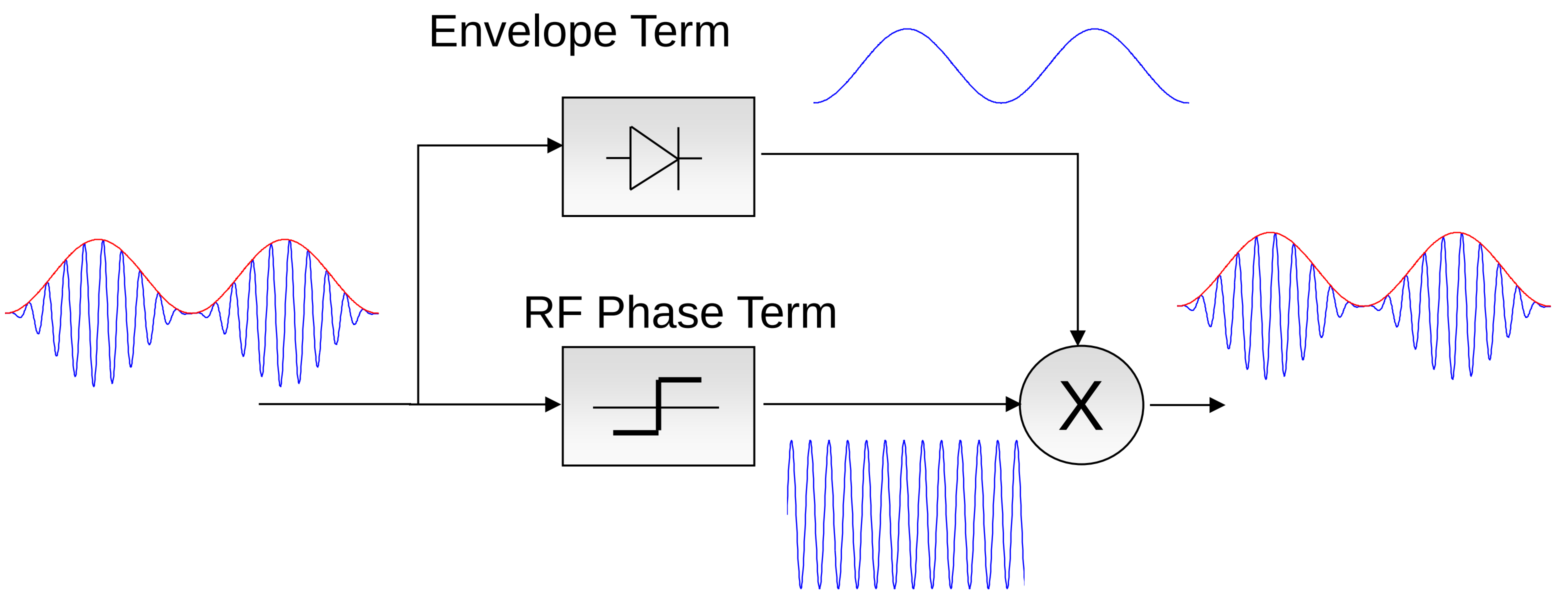
Using trig identities, y(t) can be shown to be the sum of three sine waves:

$$y(t) = A\sin(2\pi f_c t) + \frac{1}{2}Am\left[\sin(2\pi\left[f_c + f_m\right]t + \phi) + \sin(2\pi\left[f_c - f_m\right]t - \phi)\right].$$

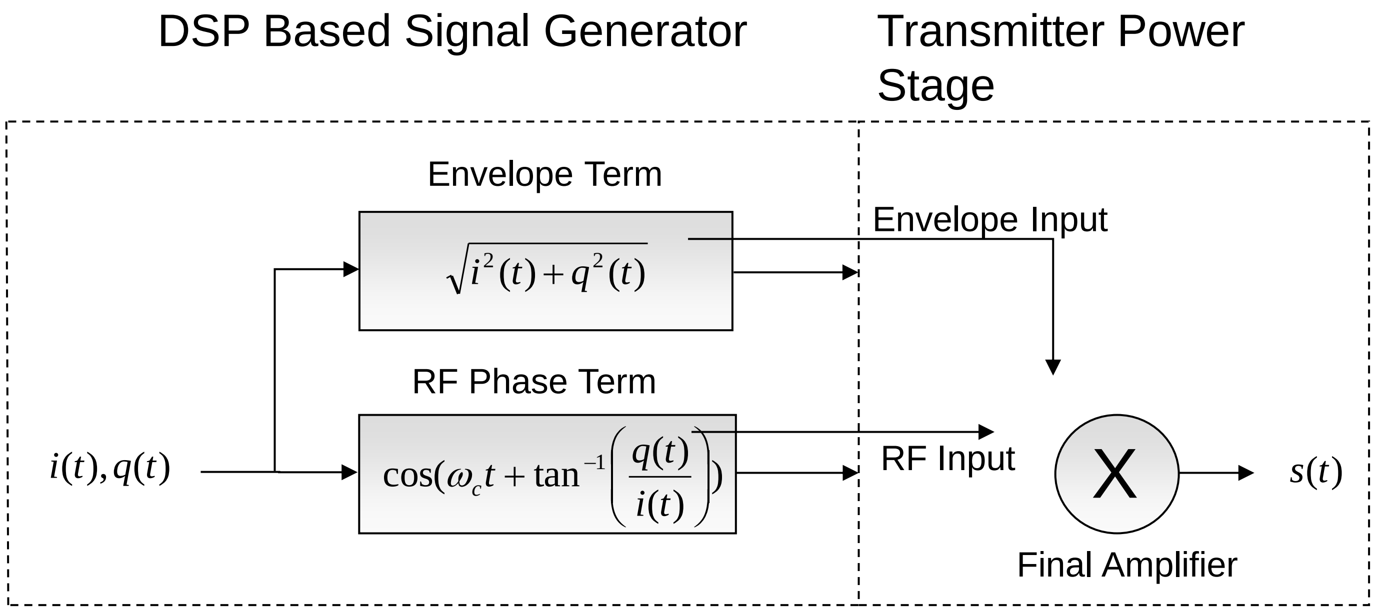
Therefore, the modulated signal has three components: the carrier wave c(t) which is unchanged, and two pure sine waves (known as sidebands) with frequencies slightly above and below the carrier frequency fc.

Modulation Design

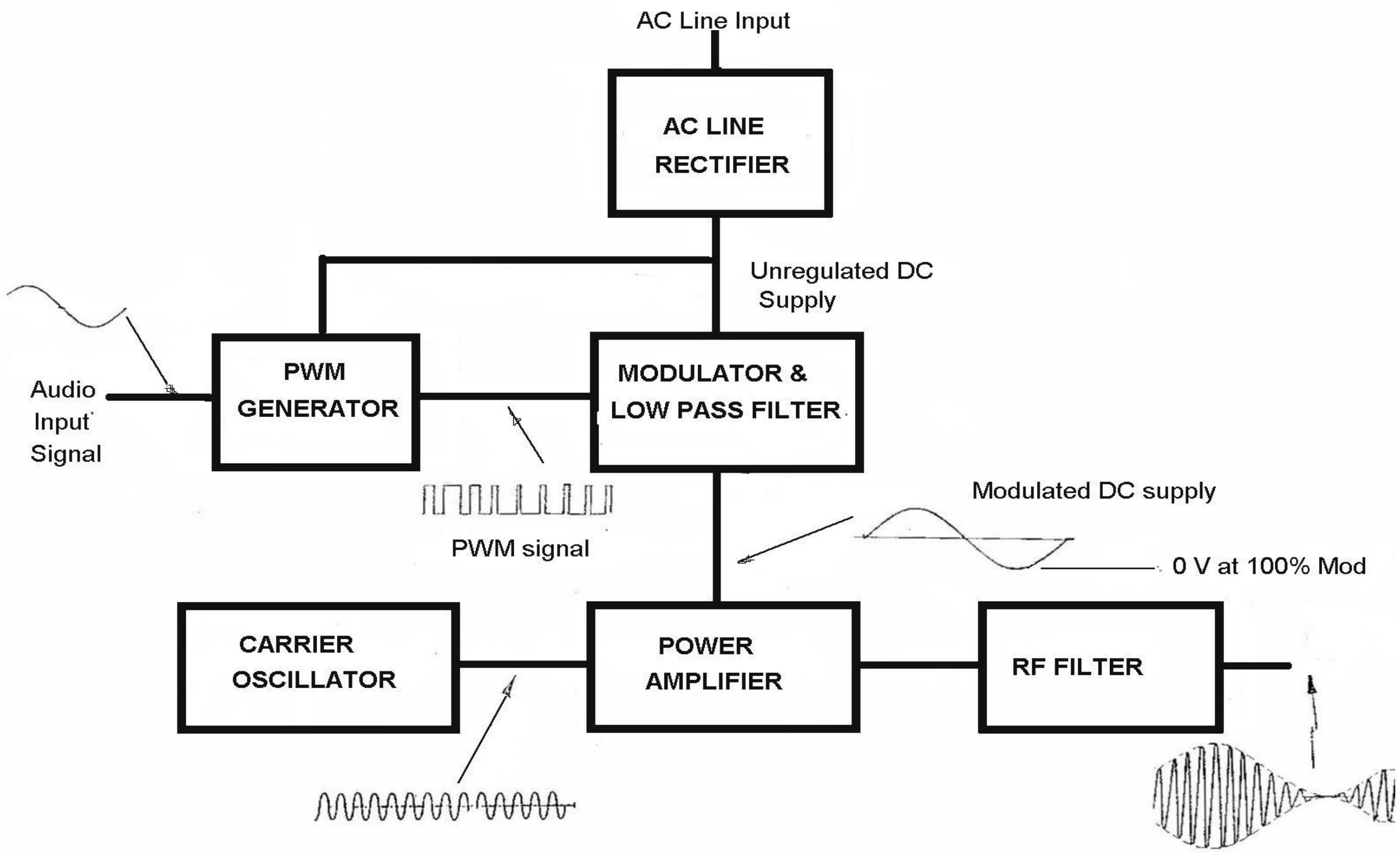
Envelope Elimination and Restoration
a.k.a. Kahn Technique



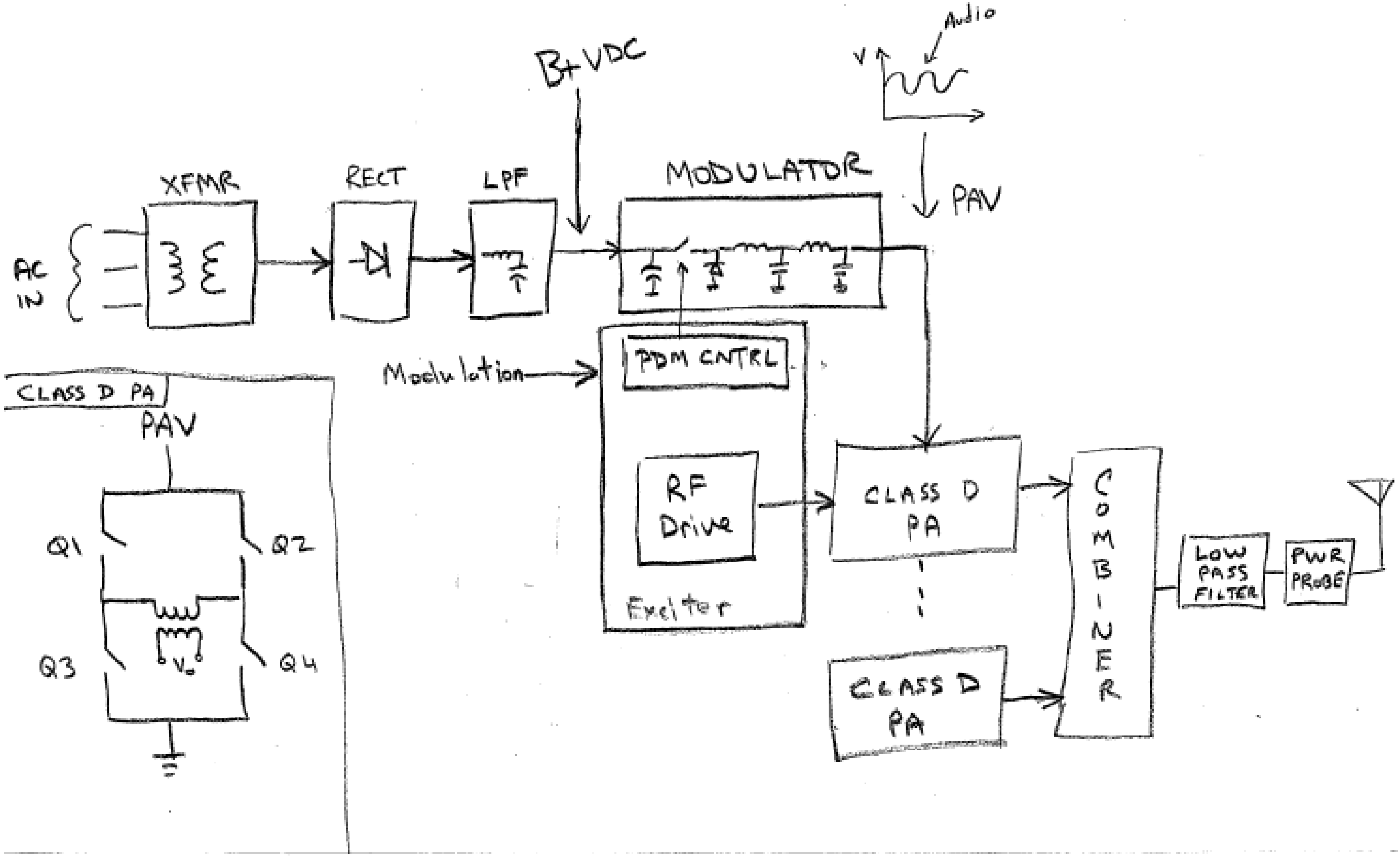
Modulation Design



AM Transmitter Block Diagram



AM Transmitter Block Diagram



RF Amplifier

The RF amplifier design is critical to the transmitter's \$/W, W/in^3, efficiency and reliability.

Usually the amplifier will be the building block of a family of models.

The power capability needs to be large enough to minimize combiner and connectors costs but small enough not to drastically affect power capability under failure. Shipping and servicing weights are also very important.

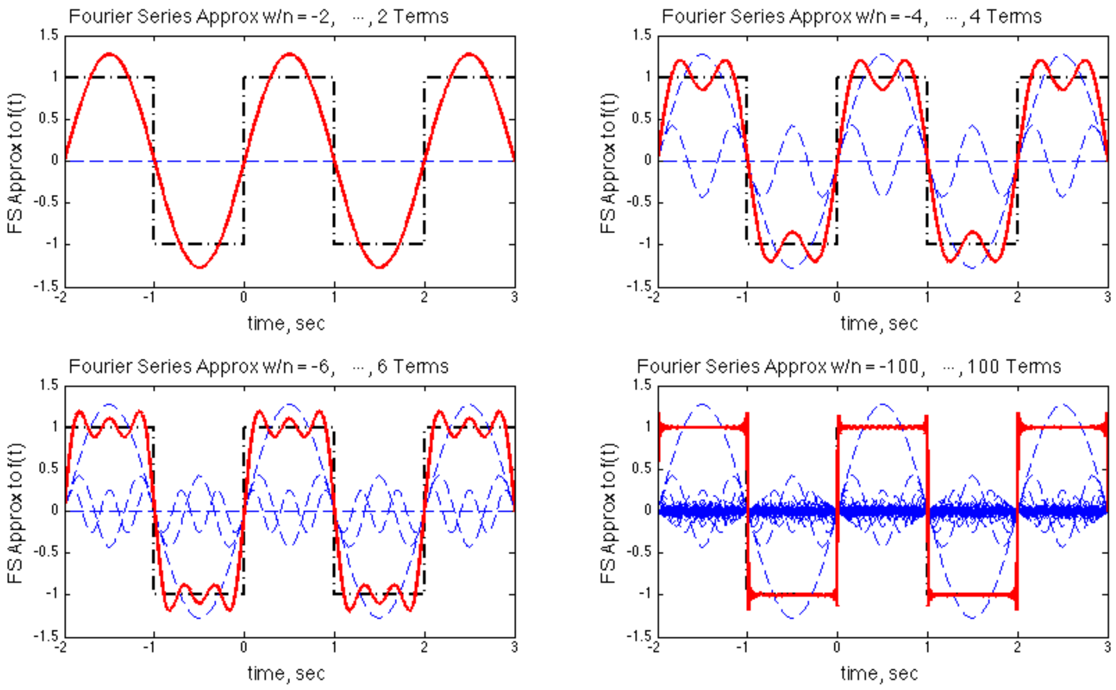
RF Amplifier

- Class D amplification has been the topography of choice since the early 1980's. Class D has excellent efficiency (theoretically 100%), good $/W and W/$\mathrm{in}^3$
- Choosing the switching device for the full bridge is critical as well.
- Drain current, input capacitance, output capacitance, dv/dt rating, thermal impedance of junction to case, case mechanics are all considered.
- The amplifier is designed always to be working into an inductive load to minimize the switching loss and dv/dt.

RF Amplifier

$$f(x) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin\left(\frac{n\pi x}{L}\right).$$

Square wave produced by Class D has a fundamental and many odd harmonics



RF Amplifier

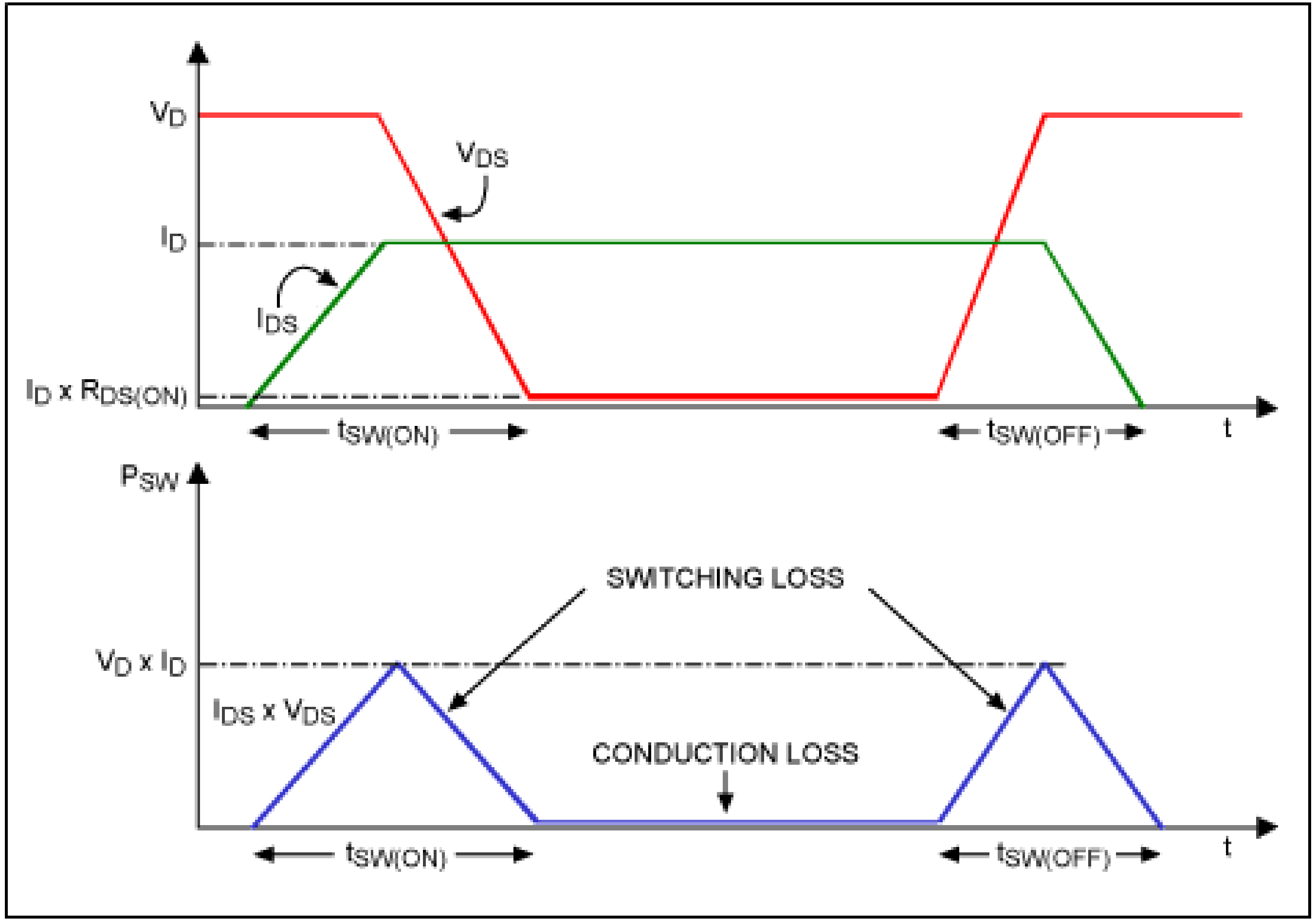
Amplifier efficiency is affected by 2 factors:

- FET on resistance (i^2R_{DSon})
- Switching loss ($1/2CV^2F$)

R_{DSon} can be minimized by choosing a high current FET

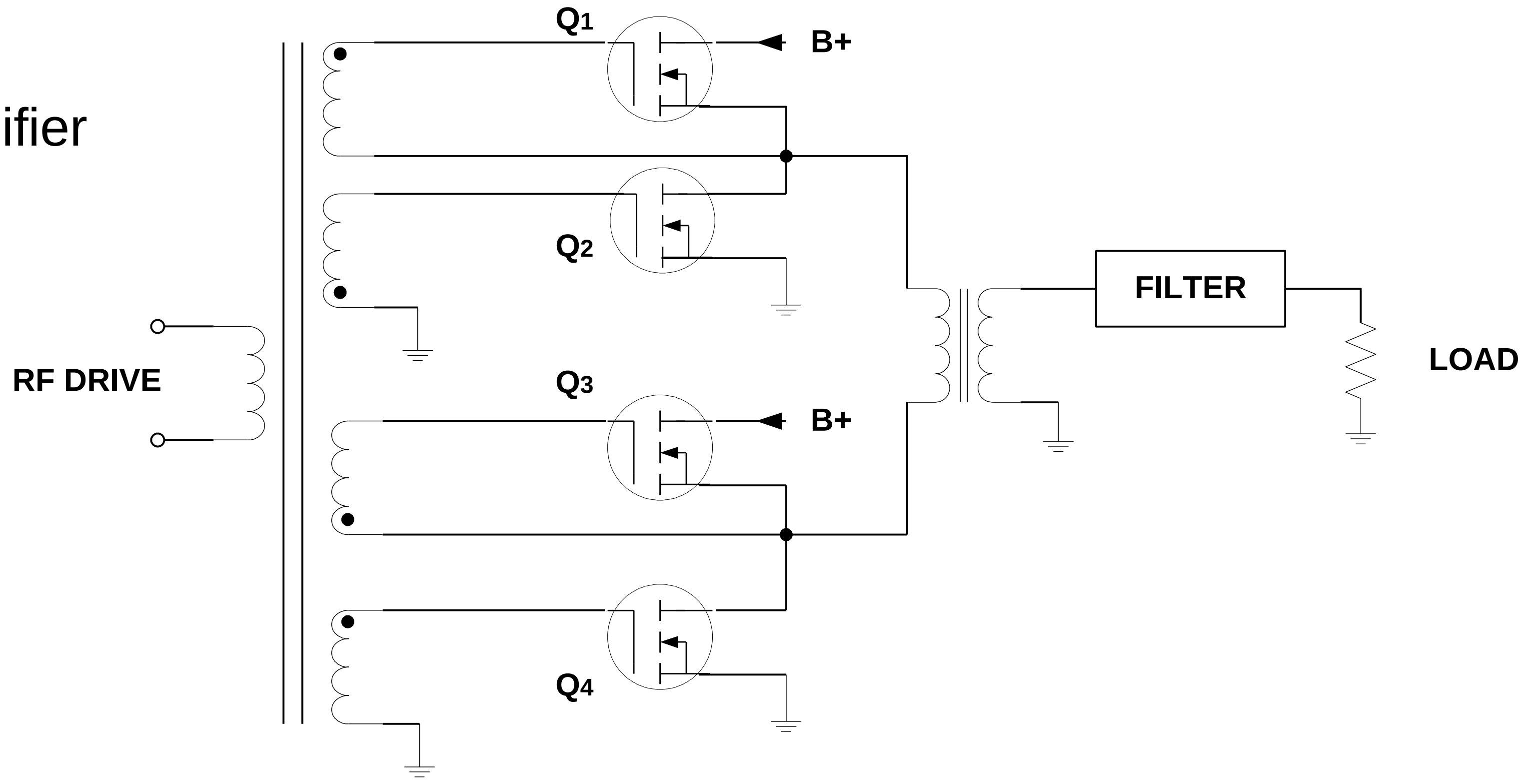
Switching loss can be minimized by reducing the voltage across the FET during turn on – this is accomplished by an inductive load also known as zero voltage switching (ZVS)

RF Amplifier



RF Amplifier

Class D Amplifier



RF Amplifier

Design sequence (iterative)

1) FET selection determines B+ (BVdss x derating)
2) Modulation depth selection determines PAV {PAV=B+/(mod+1)}
3) TX TPO and # of RF modules determine power per module
4) System impedance, # of RF modules and combiner turns ratio determines filter input impedance and PA impedance
5) Filter input impedance determines filter component values

Power = $Voltage^2$/resistance

PA testing and analysis to ensure PA power is reliable

RF Amplifier

Typical values for NX50

1) B+=400VDC
2) PAV=163VDC
3) MOD Depth =145%
4) # of RF modules =20
5) Filter input Impedance = 4.17Ω<25° or 4.60Ω//+j9.87Ω
6) Primary Turns = 6
7) PA impedance= 8.28Ω//+j17.77Ω
8) PA Power = $146V\ rms^2$/8.28Ω = 2574watts*
9) 2574watts x 20= 50kW

*don't forget square wave to sine conversion (4/π) and peak to RMS (1/sqrt2)

RF Amplifier

Engineering has designed a spreadsheet to execute the required calculations efficiently

Generalized Harmonic Filter Network - Shunt Notch

Peak Mod	PA(V) @ FP	Phase Angle	Veffective	Pout	Nominal FET Resistance (mOhm)	Rfet*2	Pfet	Rac	Pload	Efficiency	Xl	Total Rac @ 20 degrees	Primary Turns (Cube)	Secondary Turns (Combiner)	Number of Modules	Output Impedance
145.00%	163.27	25.00	133.22	2500.00	50	0.15	55.18	6.80	2500.00	0.98	3.17	7.50	6	1	20	50

Frequency		Input Impedance per Input				Inputs	Power per Input		Total Power (kW)		
kHz	rad/s	R	+JX	mag	phase	n	RMS	Peak	RMS	Peak	Carrier
1710	1.1E+07	3.78	1.76	4.2	25.0	1	75000	300125	75	300.125	50

Resistances		Elementary 90 Degree T Section Impedances										
Resistance		Phase	First T			Second T			Series Capacitor		Shunt Notch	
Input	Centre	L1a (uH)	Z1	L (uH)	C (nF)	Z2	L (uH)	C (nF)	Cs (Ω)	L3b (uH)	C2n (nF)	Ln (uH)
3.78	13.7	0.164	7.20	0.67	12.92	26.2	2.44	3.55	30	2.79	3.16	0.305

Adjusted Centre Resistance

13.739

Centre Resistance Adjustment Factor

1

Note: decrease if measured capacitance is > 100% by 0.01 at a time until all inductors are calculated and then decrease by an additional 0.03. Confirm Voltage is less than 66%, Current is less than 70% and Power is less than 66% of rated for all capacitors

Ideal Network (90 Degree T Sections)							
Capacitors (nF)			Inductors (uH)				
C1	C2	Cs	L1 (ttl)	L1 (per)	L2	L3	Ln
12.92	3.16	3.102	0.834	0.83	3.110	5.23	0.3049

Stress Levels - Ideal Network														Normalized Stress Levels					
Power (kVAR)			Current (rms Amps)								Voltage (peak)			Power (kVAR per nF)			Current (rms Amps per nF)		
C1	C2	Cs	C1	C2	Cs	L1 per	L1 total	L2	L3	Ln	C1	C2	Cs	C1	C2	Cs	C1	C2	Cs
182	205	45	159	83	39	140.9	141	74	39	83	3242	6959	3287	14.1	65.0	14.5	12.3	26.4	12.5

Reduced Q Network						
Measured Capacitance (nF)			New Required Inductance (uH)			
C1	C2	Cs	L1 (ttl)	L2	L3	Ln
12.00	3.00	3.00	0.75	2.36	3.93	0.32
93%	95%	97%	89%	76%	75%	105%

Increased Q Network for First T Section						
Inductance (uH)		C1	C1 Stress			
L1 (ttl)	L2	nF	kVAR	kVAR/nF	Irms	Vpk
1.03	3.38	12.00	256.4	21.365	181.81	3989.3
123%	109%	93%	141%	151%	114%	123%

Stress Levels - Reduced Q Network														Normalized Stress Levels - Reduced Q Network					
Power (kVAR)			Current (rms Amps)								Voltage (peak)			Power (kVAR per nF)			Current (rms Amps per nF)		
C1	C2	Cs	C1	C2	Cs	L1 per	L1 total	L2	L3	Ln	C1	C2	Cs	C1	C2	Cs	C1	C2	Cs
136	161	47	133	72	39	141	141	74	39	72	2910	6316	3399	11.4	53.6	15.5	11.1	24.0	12.9
75%	78%	103%	83%	86%	100%	100%	100%	100%	100%	86%	90%	91%	103%	81%	82%	107%	90%	91%	103%

Loaded Q of L Sections				Phase of L Sections				+JX Phase
T1-in	T1-out	T2-in	T2-out	T1-in	T1-out	T2-in	T2-out	
1.65	0.16	1.68	0.22	59	9	59	13	25

C1	C2	Cs	L1	L2	L3	Ln	
136	161	47	-97	138	63	18	kVar
1200	1200	1200	1000	1000	1000	500	Q
114	134	39	-97	138	63	36	Watts

Total Watts	427
Efficiency	99.43%

Total Phase Delay (With Input Term): 165

Total Calibration Phase Delay: 140

NG200, Zin: 13.4 + J3.7, 300 kW average, 1110 kW peak

Note: Requires series pairs for C2, Cannot use CS45 except for Cs

RF Amplifier

FET chosen for NX

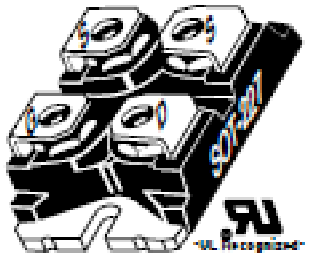
ADVANCED POWER TECHNOLOGY®

APT50M50JFLL

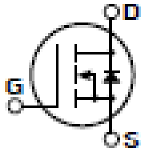
500V 71A 0.050Ω

POWER MOS 7® FREDFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g. Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Qg
- Increased Power Dissipation
- Easier To Drive
- Popular SOT-227 Package
- FAST RECOVERY BODY DIODE



RF Amplifier

MAXIMUM RATINGS All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT50M50JLL	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ T_C = 25°C	71	Amps
I_{DM}	Pulsed Drain Current ①	284	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ T_C = 25°C	595	Watts
	Linear Derating Factor	4.76	W/°C
T_J,T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ① (Repetitive and Non-Repetitive)	71	Amps
E_{AR}	Repetitive Avalanche Energy ①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ④	3200	

RF Amplifier

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage (V_{GS} = 0V, I_D = 250µA)	500			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ② (V_{GS} = 10V, 35.5A)			0.050	Ohms
I_{DSS}	Zero Gate Voltage Drain Current (V_{DS} = 500V, V_{GS} = 0V)			100	µA
	Zero Gate Voltage Drain Current (V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C)			500	
I_{GSS}	Gate-Source Leakage Current (V_{GS} = ±30V, V_{DS} = 0V)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 5mA)	3		5	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - http://www.advancedpower.com

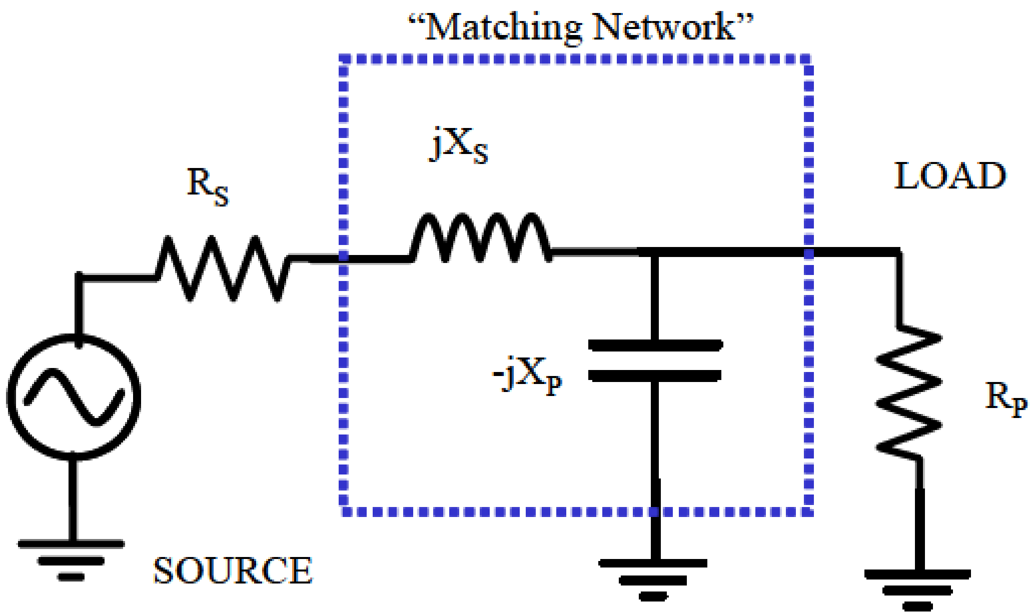
Harmonic Filter

Harmonic filter needs to impedance match the antenna to the amplifier to achieve designed power. (4.17Ω<25° to 50 Ω)

The harmonic filter needs to attenuate harmonics produced in the amplifiers.

The harmonic filter needs to provide isolation from external energy which could damage the amplifiers.

Harmonic Filter



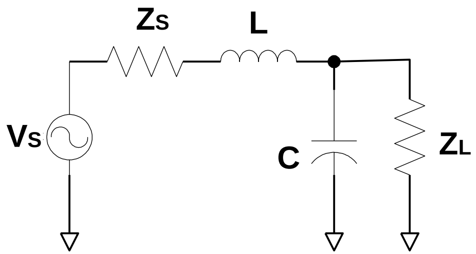
$$X_S = Q\,R_S$$

$$X_P = R_P / Q$$

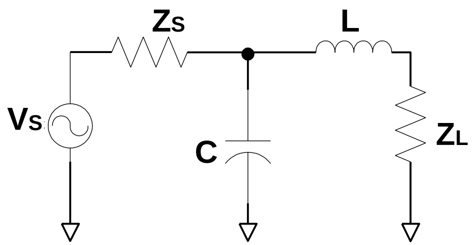
We can know Q because: $Q^2 + 1 = \frac{R_P}{R_S}$ or $Q = \sqrt{\frac{R_P}{R_S} - 1}$

Harmonic Filter

L Networks are used to step up or step down impedance

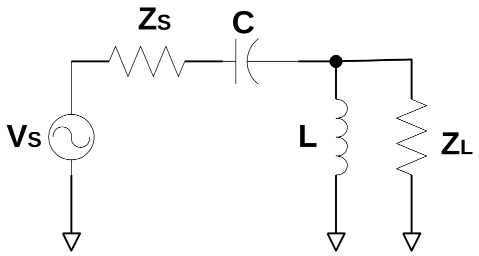


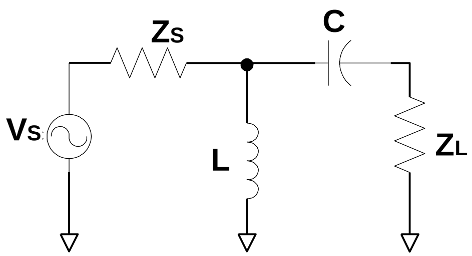
(low to high Z)



(high to low Z)

Low-pass

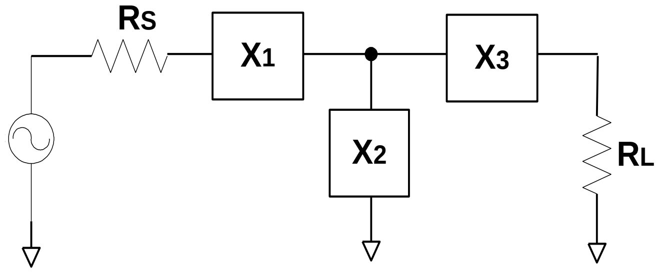




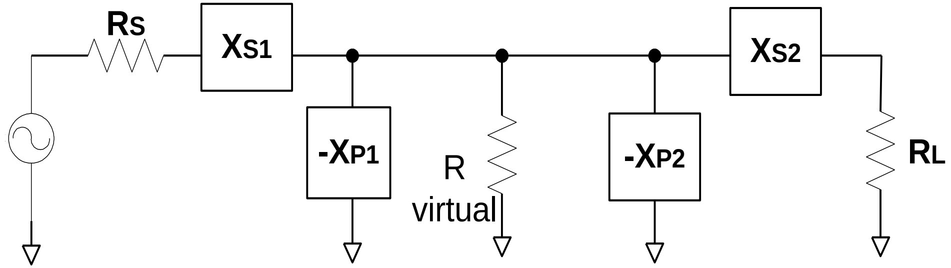
High-pass

Harmonic Filter

T networks are back to back L networks



Three-element T Network



Harmonic Filter

Harmonic filter uses a double Tee with 3rd notch design to reduce harmonics and impedance match the RF amp to the antenna. Double Tee has the advantage of :

- keeping impedance matched as shunt C drifts with temperature
- Wide bandwidth
- Good attenuation

A series capacitor and shunt coil provide static and low freq transient protection as well as transient suppressor device.

Combiner

The combiner needs to efficiently add the RF modules powers while providing isolation between inputs.

Combiners can be categorized as those with balancing resistors and those without.

Number of inputs needs to be greater than 4 for combiners without balancing resistors in ordered for reasonable isolation under failure.

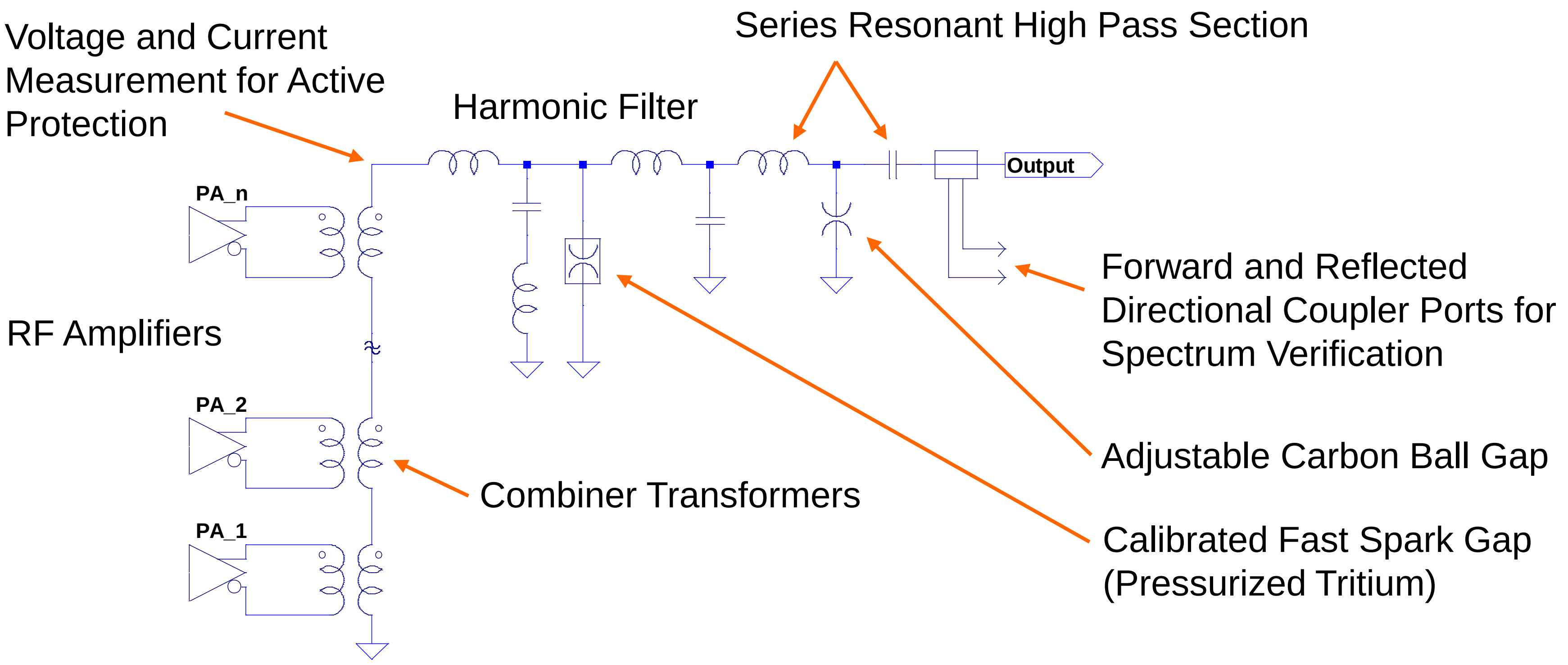
Combiner

AM, for several generations, has used combiners without balancing resistors.

AM Combiners have been both parallel (60°) and series.
Ampfet , NX = series
ND, XL, XR, NA= parallel

Series combining is broadband, less expensive, and uses a smaller footprint

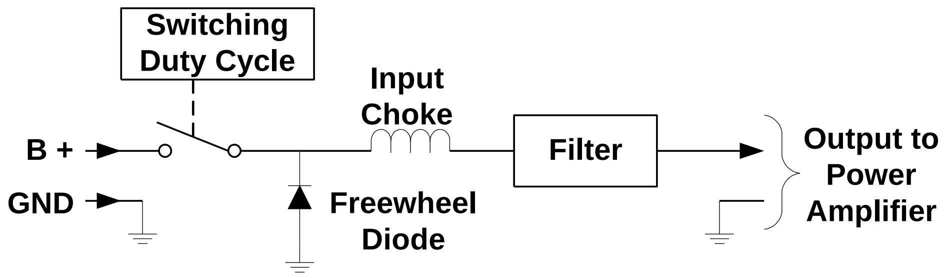
Combiner/Harmonic Filter



Frequency Agile: Harmonic Filter Re-Tune in a Few Hours

Modulation Design

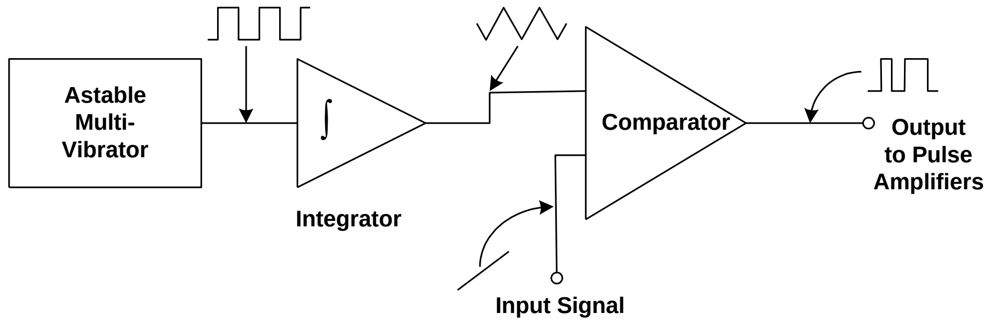
Pulse Width Modulator



- This circuit illustrates the simple switched modulator principle. It applies a fixed DC supply voltage B+ through a series switch to a low pass filter.
- The switch is opened and closed at a fixed frequency of approximately 70kHz producing a square wave with a peak value of B+ at the filter input.
- The filter rejects the 70kHz signal and produces a dc voltage at its output equal to the average value of the square wave
  - Example: one half of B+ for a 50/50 duty cycle.
- If the duty cycle is slowly varied, the DC output voltage may be adjusted from 0 to B+.

Modulation Design

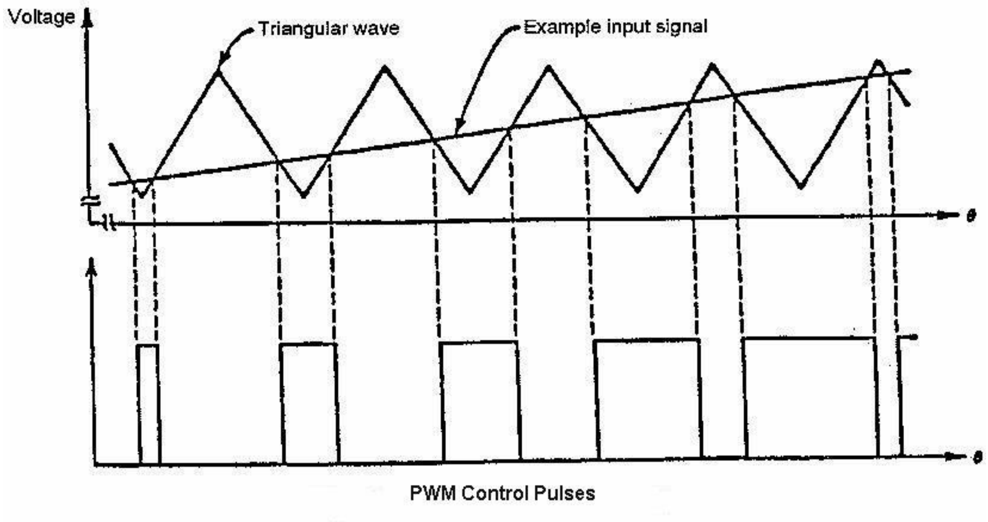
Origins of PWM Generator



- 70kHz multi-vibrator can be passed to an integrator to produce the required saw-tooth waveform.
- If an audio modulating signal is superimposed on the control voltage, then the width of the pulses in the PWM control signal will vary accordingly.
- Waveforms depicting this process are shown on the next slide.
- It is important to understand that both the RF output level and the modulation information is digitally encoded into the PWM control signal's pulse width while its repetition frequency and amplitude remain constant.

Modulation Design

PWM Generator Waveforms

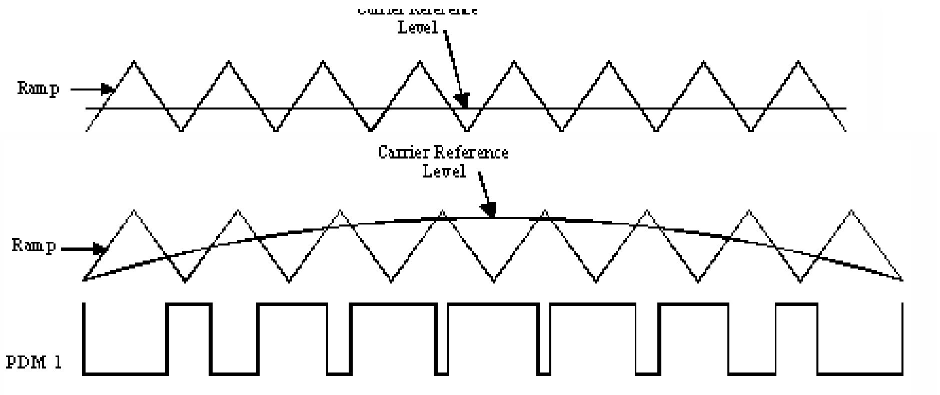


- These waveforms illustrate how the width of the PWM pulses increase in response to a rising control waveform input.
- Note the constant amplitude and repetition frequency of the PWM signal.
- The saw-tooth must have a very stable DC reference level and a very linear slope to ensure high fidelity of the transmitter's modulated output signal.

Modulation Design

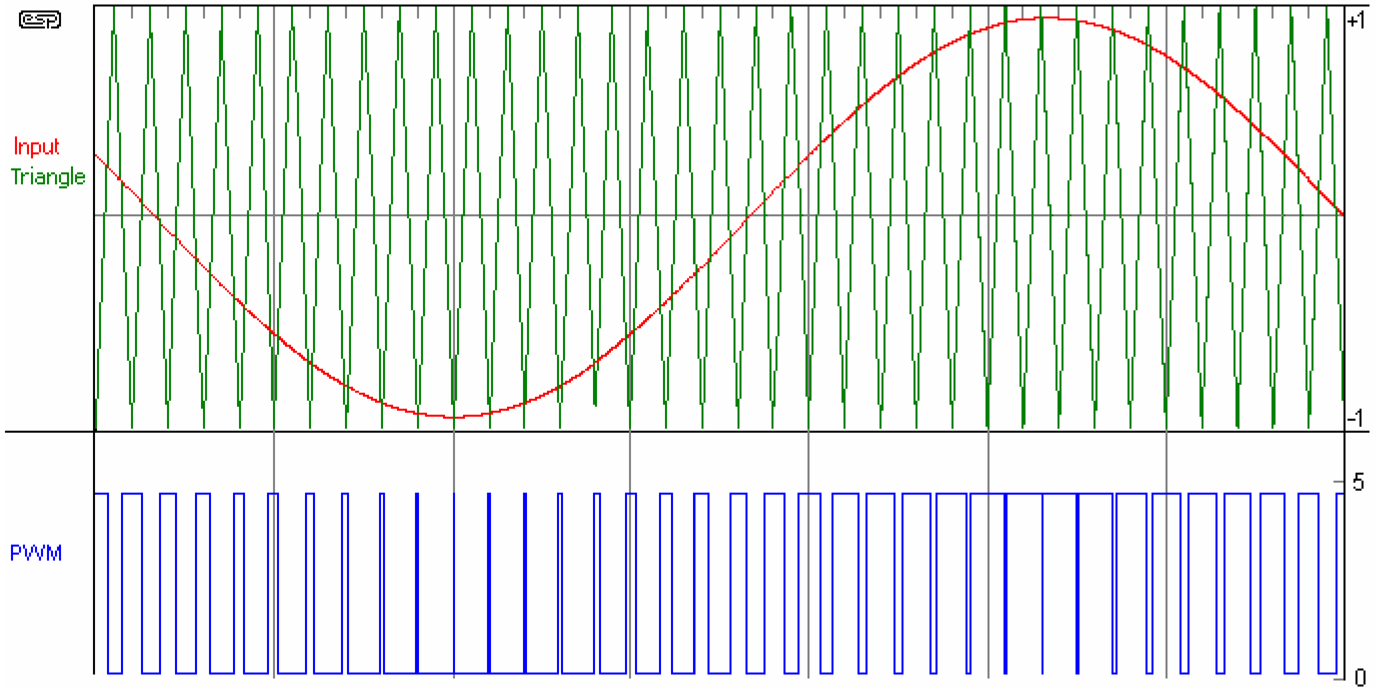
- PWM signals generated for Carrier only – no audio applied

- PDM signals generated for carrier with audio applied



Modulation Design

- PWM signals generated for Carrier only – no audio applied
- PDM signals generated for carrier with audio applied



Modulation Design

Digital Modulation Technology

Separate power processing stages for Envelope Modulation and RF Amplification are Employed. This approach enjoys the following benefits:

- Optimal RF Transistor switching is maintained at all modulation levels. This cannot be achieved when the RF transistors must both convert DC to RF and vary the RF envelope.
- Digitally controlled RF Transistor switching has nearly eliminated switching loss across the AM band
- Allows for very high current capability transistors to reduce conduction loss
- Results in ultra high efficiency RF amplifier (up to 98% at 1710 kHz)
- RF Amplifier DC Supply can be shut down during transient events/VSWR to further improve robustness
- All amplifiers see the same load at all power and modulation levels

Modulation Design

The 9 Modulation phases are separately synthesized digitally at 317 MSPS in the exciter FPGA. This results in very low quantization noise.

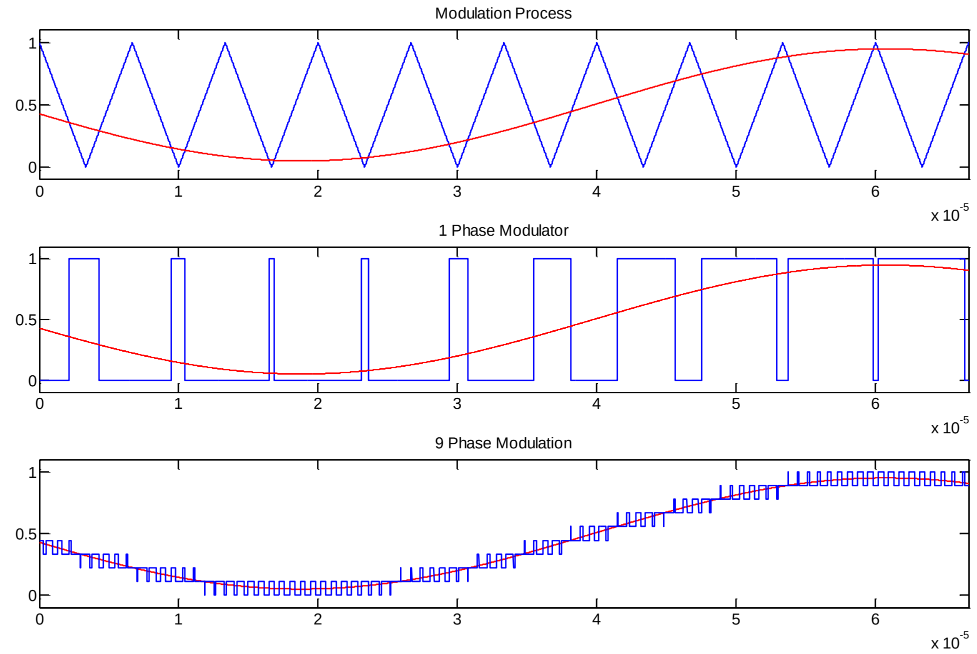
Each Modulator phase samples the desired envelope at a rate of over 300 kHz.

The 9 Phase process samples the envelope at over 2.7 million samples per second. This rate does not change with frequency.

Distortion due to the modulation process is essentially eliminated.

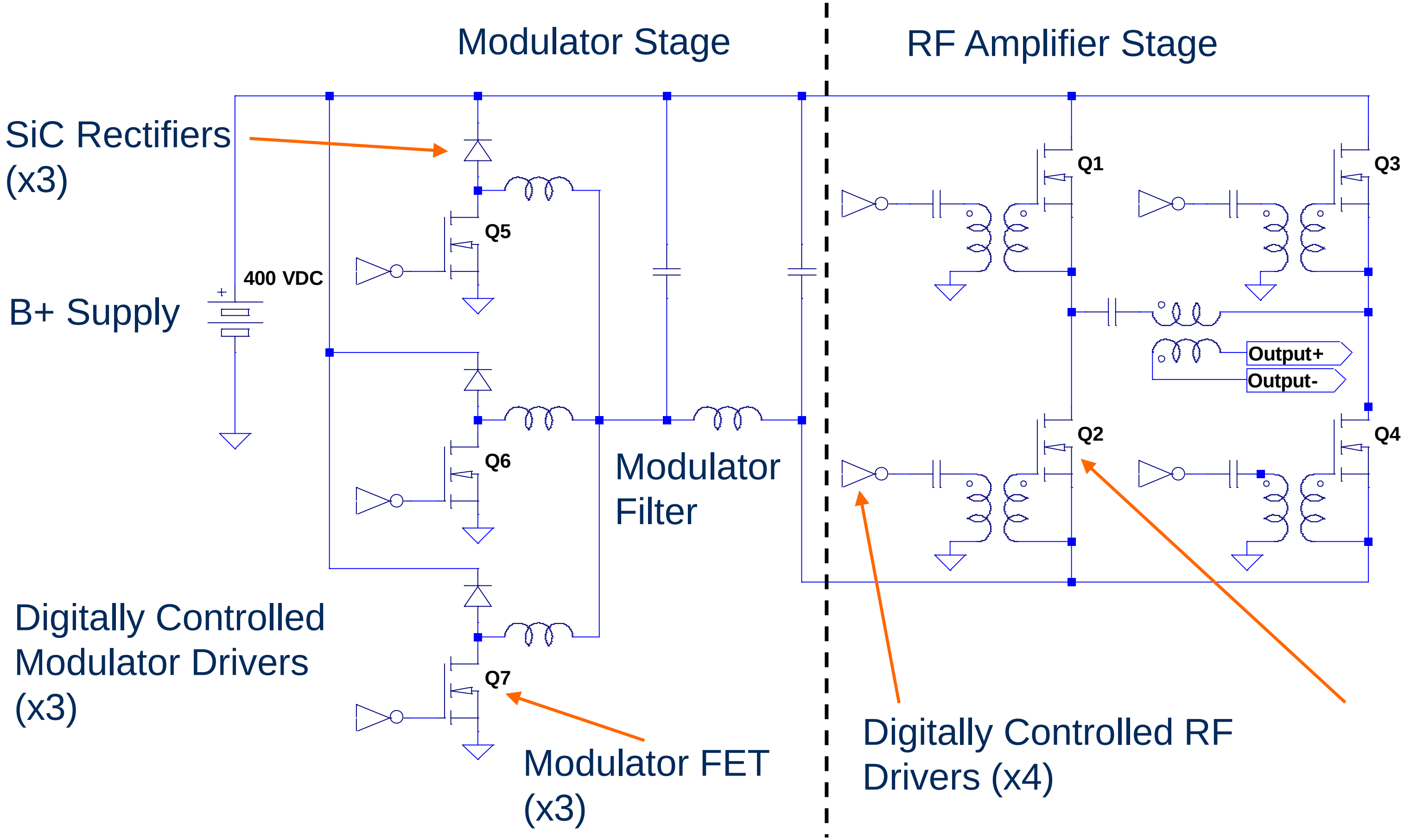
Reduced switching harmonic content allows for a very low Q modulation filter.

9 Phase Digital Modulation



Modulation Design

- Amplifier Design



Exciter

Exciter design has advanced greatly from early TTL and discretes to a powerful DSP and FPGA.

The 2 signals being generated have not changed: RF drive (carrier freq) and Mod Drive (PDM)

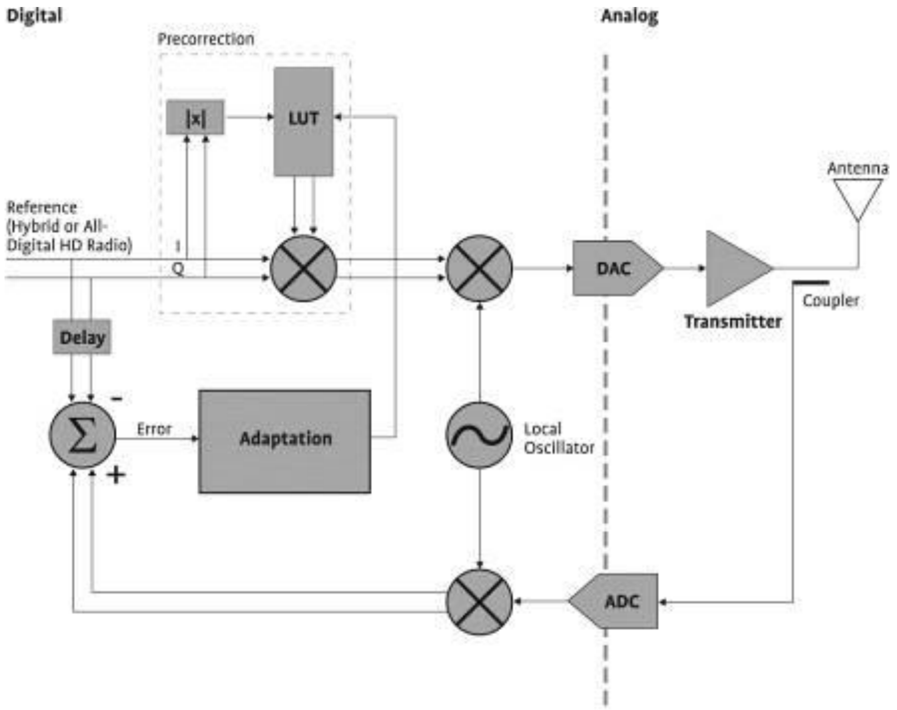
With the DSP, the exciter can now compensate for many of the distortions in the amplifiers and modulators.

Modulator pinch-off, modulator filter roll-off and RF amplifier incidental phase modulation are all corrected.

Exciter

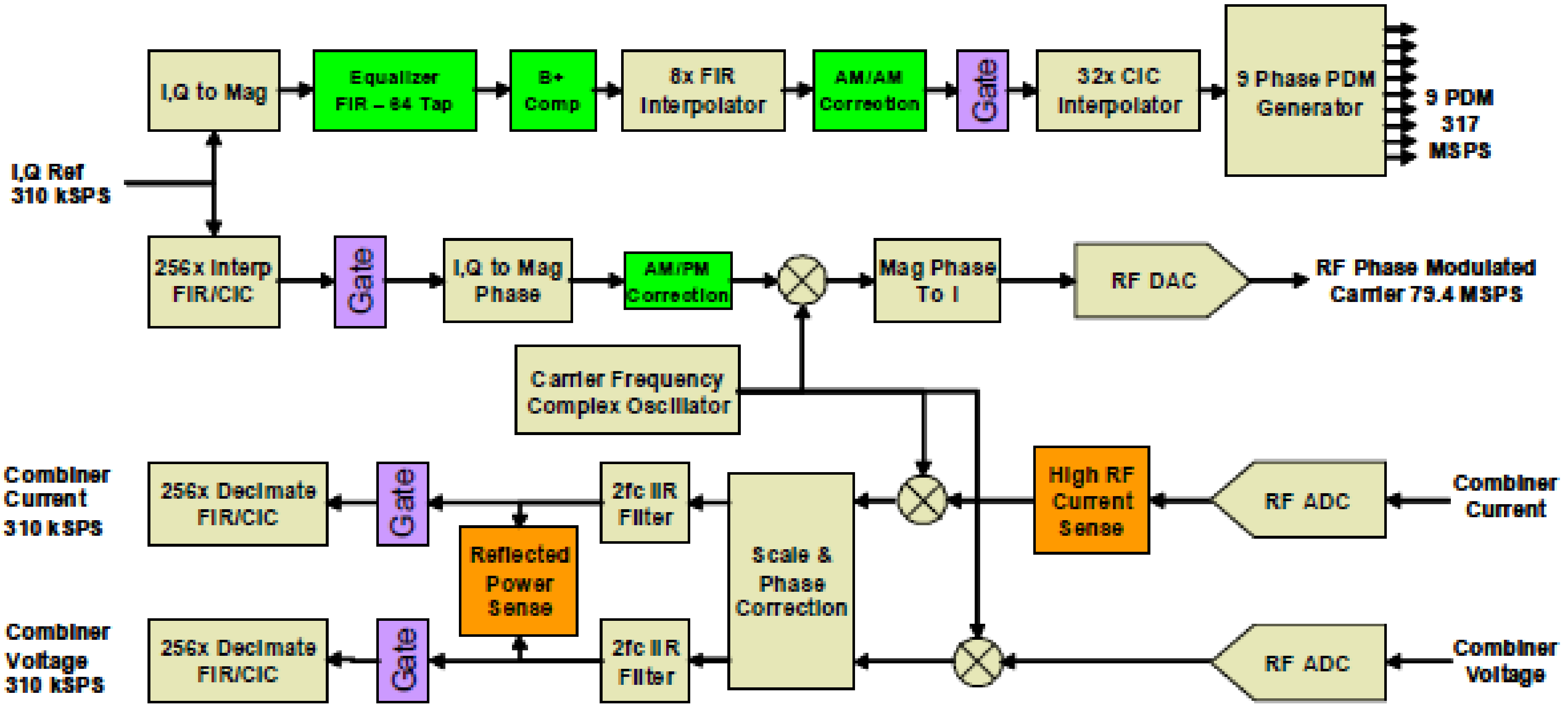
“The NX Series of AM transmitters are the first high power AM transmitters to be provided with Dynamic Pre-correction”

- Corrects primary forms of distortion
- Applies to analog + digital broadcasting
- More Linear – Clean Spectrum
- Adaptive envelope equalization
- Adaptive AM-AM correction
- Adaptive AM-PM correction



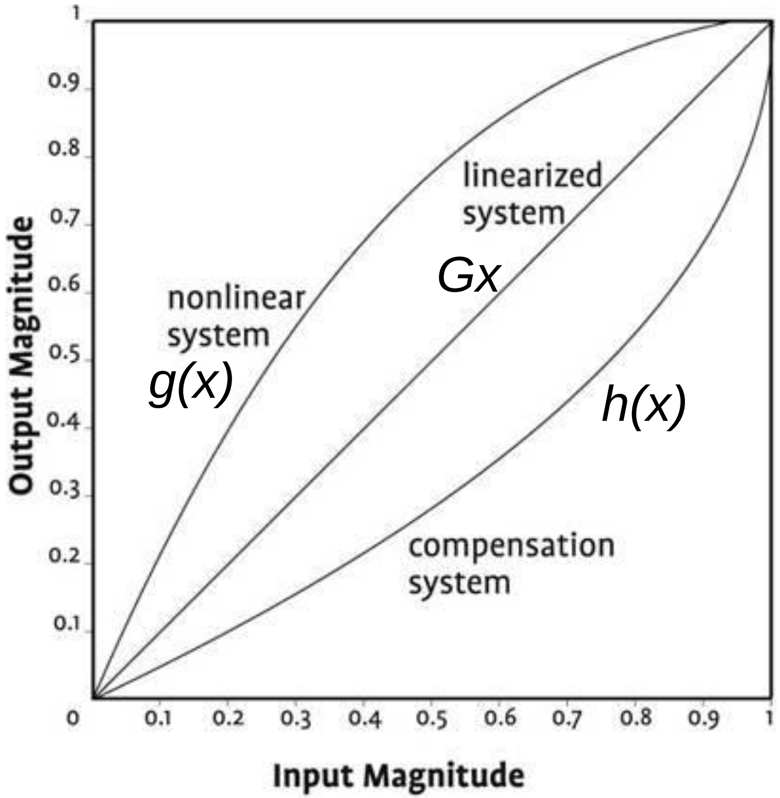
Exciter

Figure 2.2: Block Diagram - FPGA



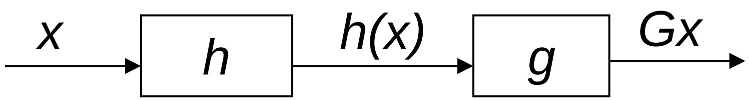
Exciter

Pre-Correction Principle



An amplifier characteristic $g(x)$ may be corrected for with a complementary characteristic $h(x)$ such that $g(h(x)) = Gx$

For this to be true, $G\,h(x) = g^{-1}(x)$



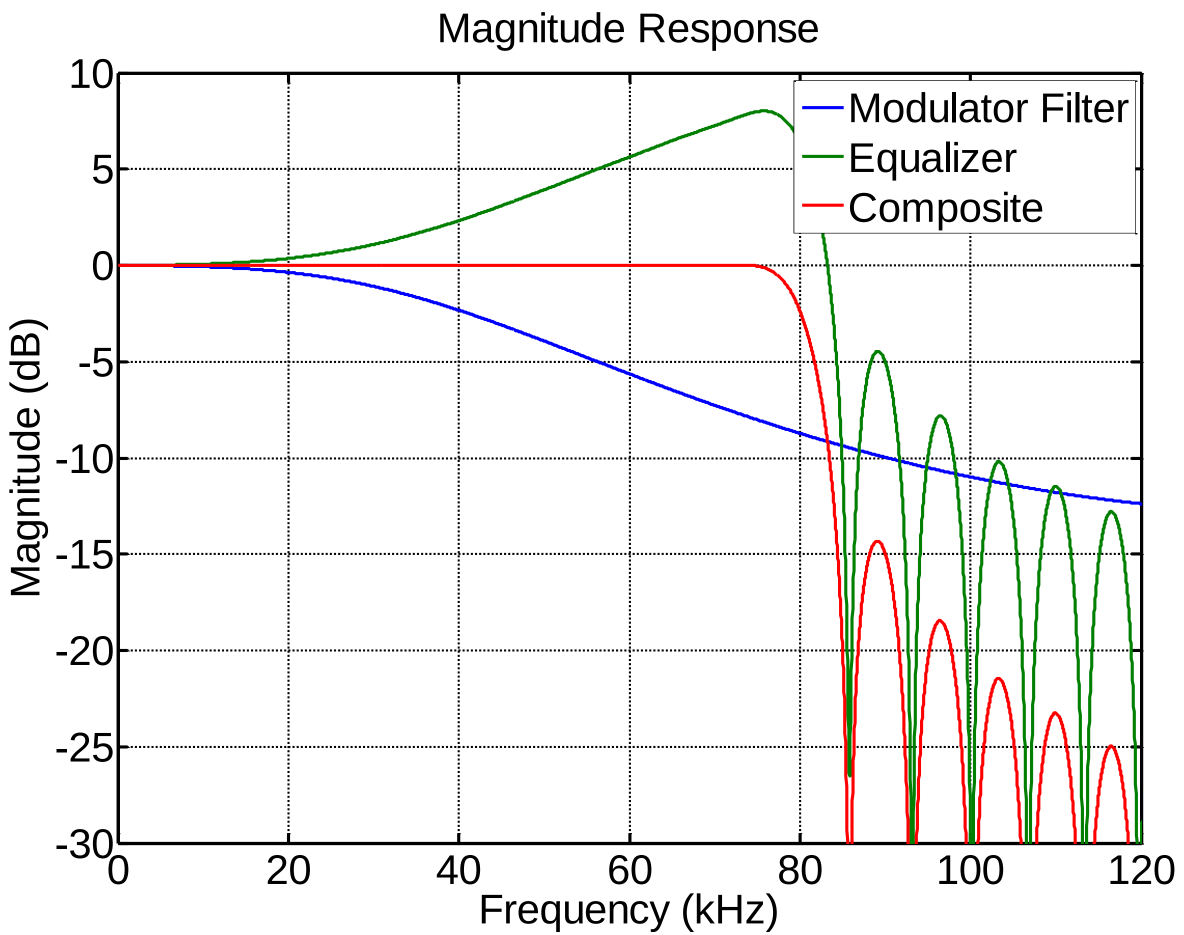
Exciter

The FPGA has three correction sections in the forward path:

- Envelope equalization: Corrects for filtering effects in the modulator (envelope magnitude and phase response versus frequency)
- AM/AM Correction: Corrects for amplitude error in the modulator due to capacitive effects in the modulator FET. (Essentially AM distortion)
- AM/PM Correction: Corrects for phase error in the RF amplifier due to capacitive effects in the RF FET. (IQM or IPM effects)

Additionally it will be possible to correct for linear effects in the AM antenna system using a filter in the DSP

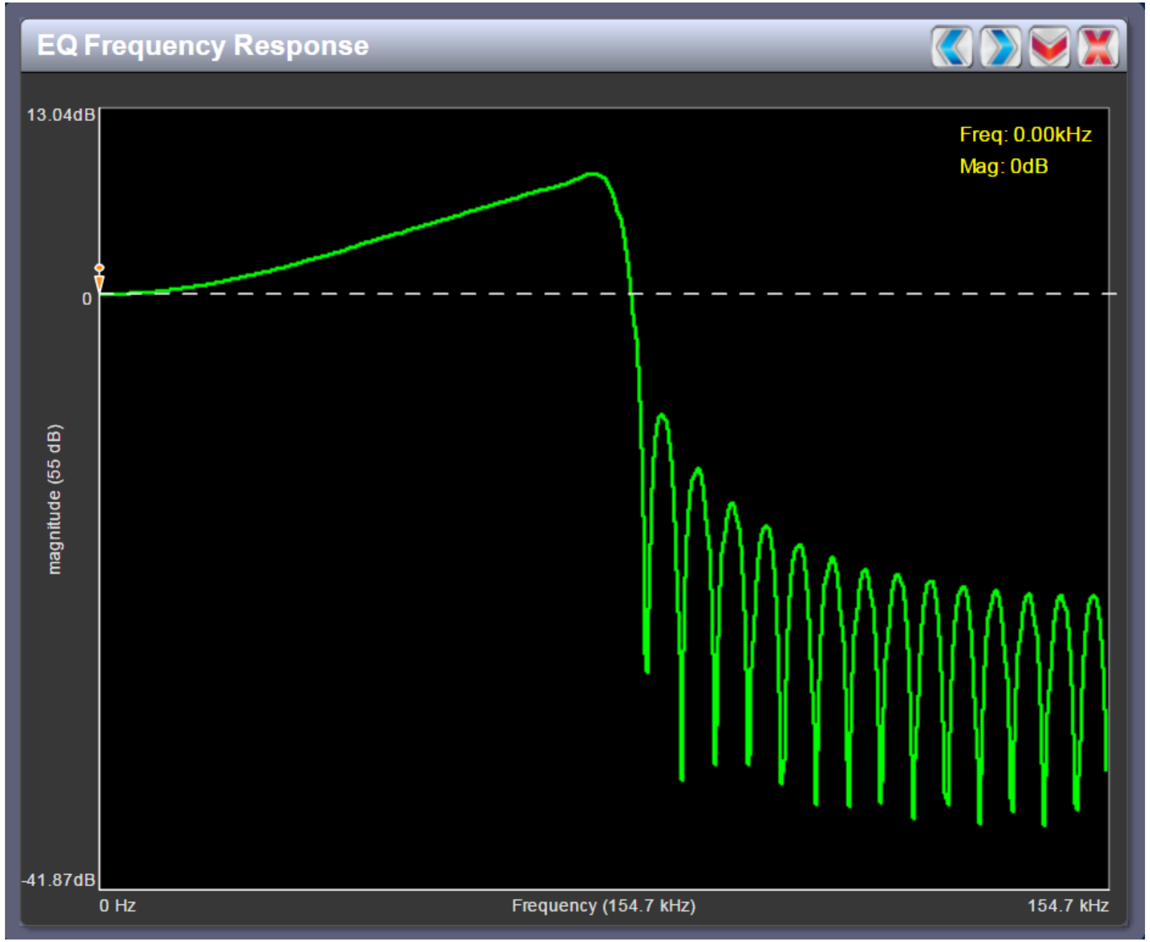
Exciter



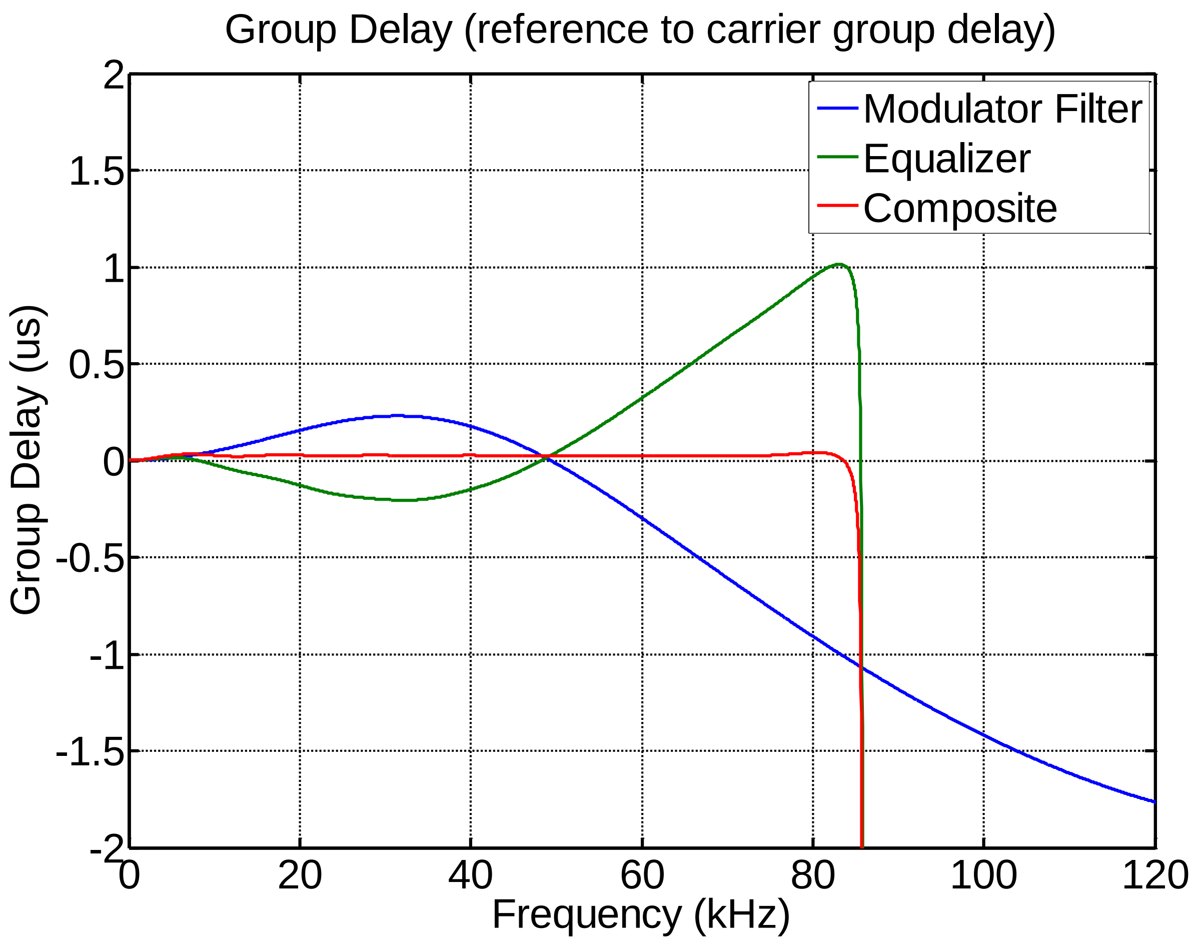
NX Modulator Response

Exciter

AUI Screen
EQ Frequency
Response



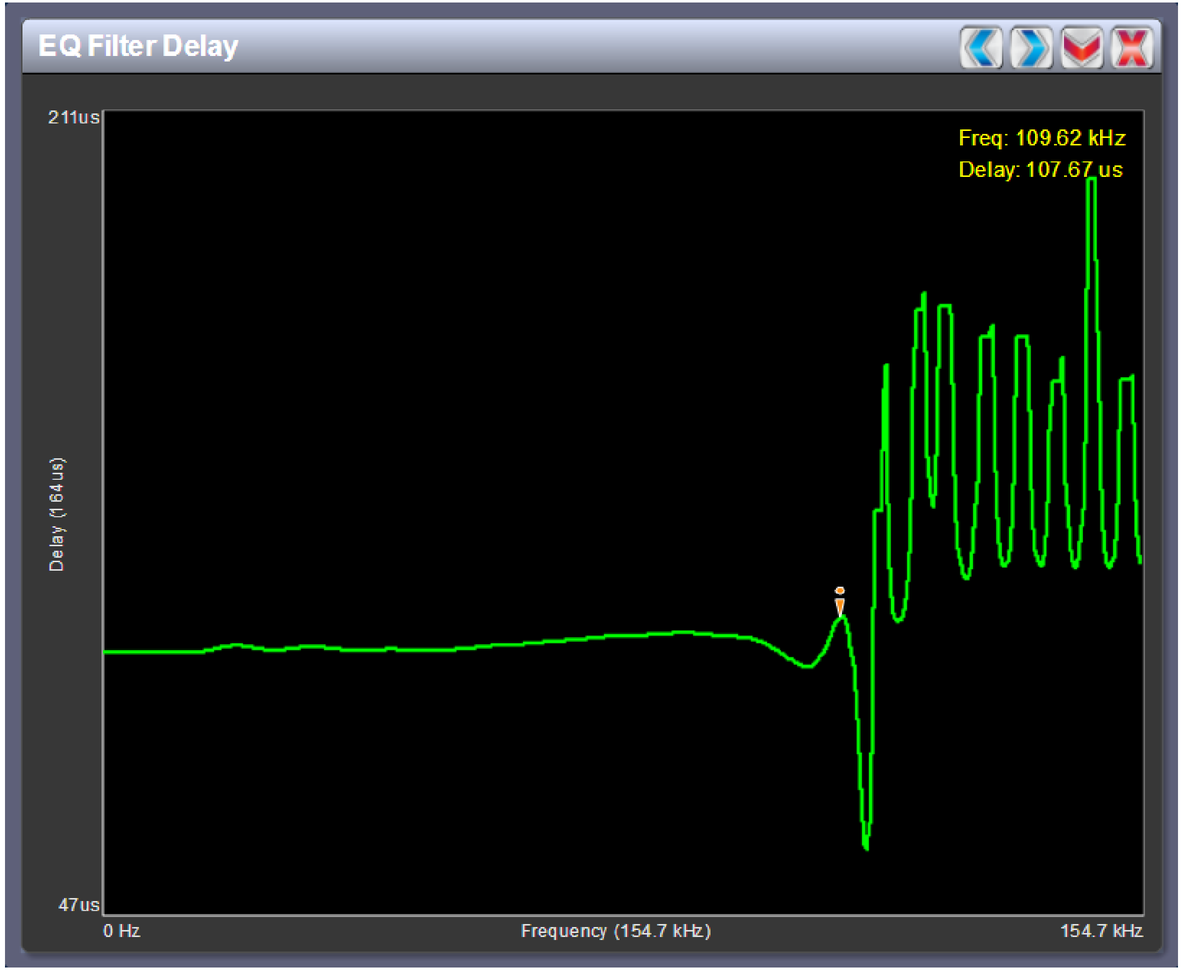
Exciter



Group Delay (reference to carrier group delay)
Modulator Filter
Equalizer
Composite
Group Delay (us)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
0
20
40
60
80
100
120
Frequency (kHz)

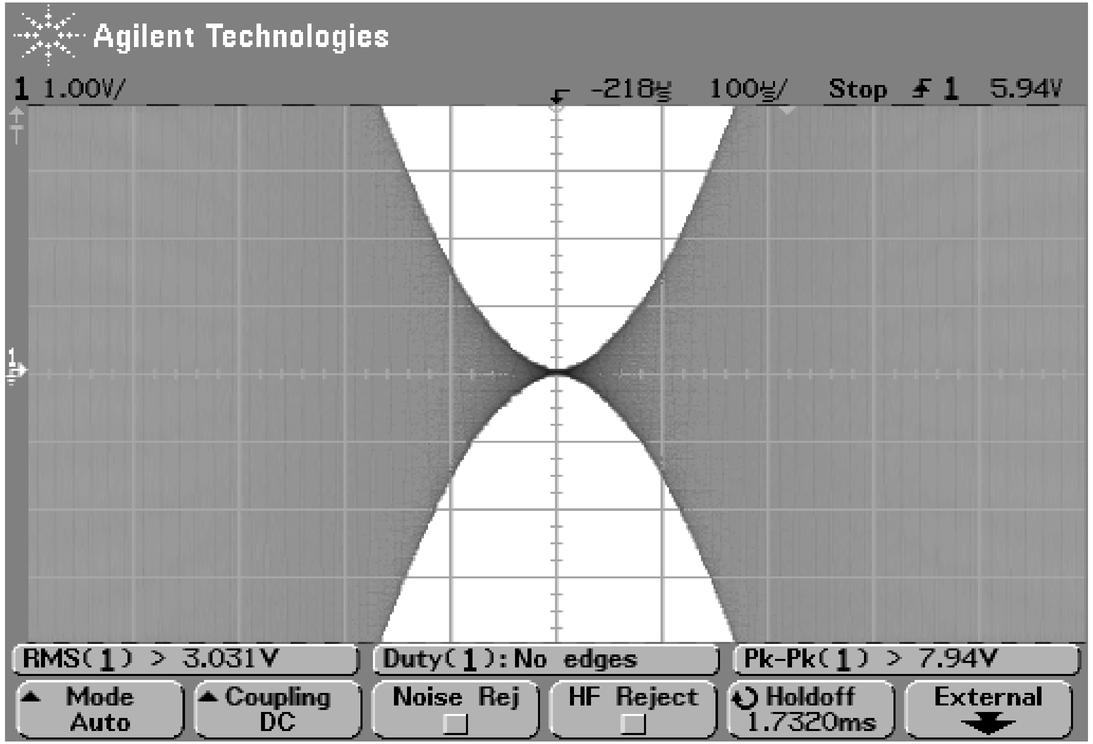
Exciter

AUI Screen
EQ Filter
Delay



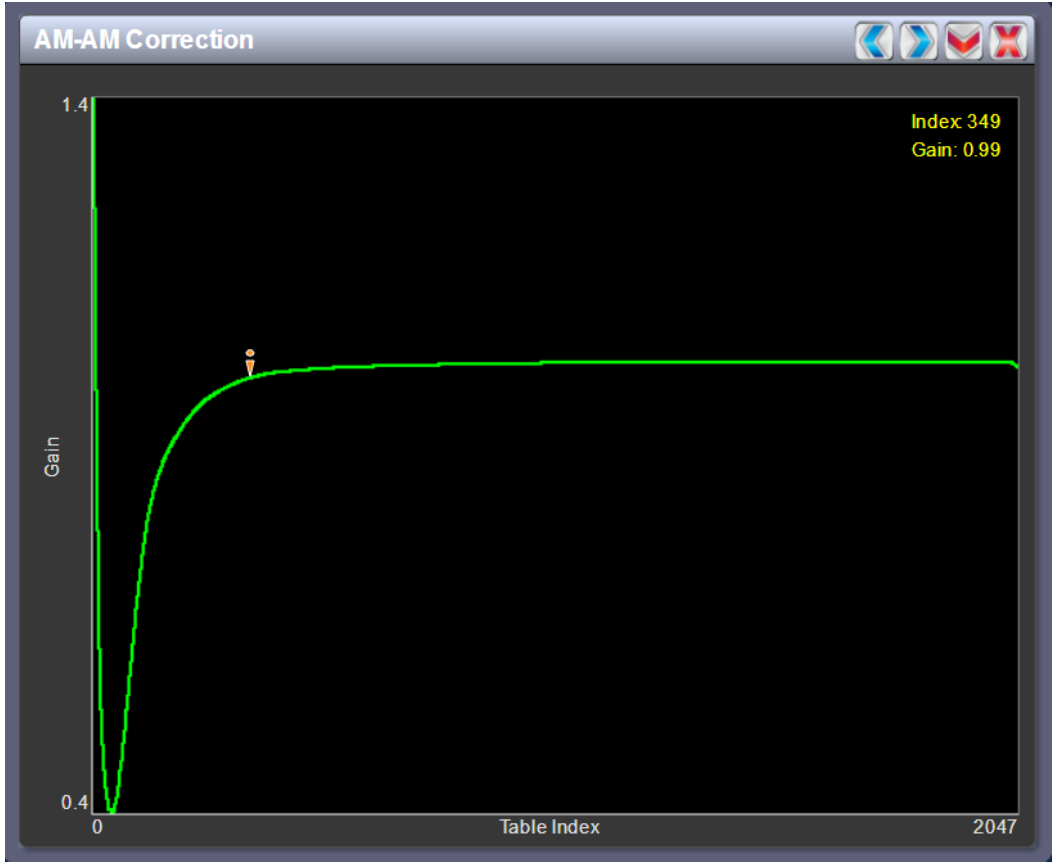
Exciter

No visible distortion in the trough with AM to AM correction



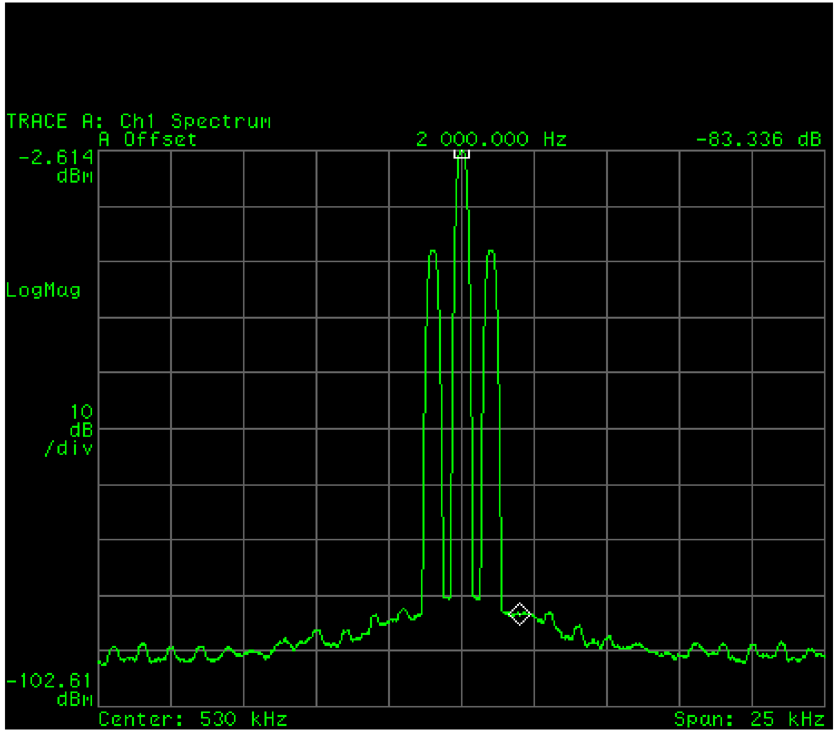
Exciter

AUI Screen
AM-AM
Correction



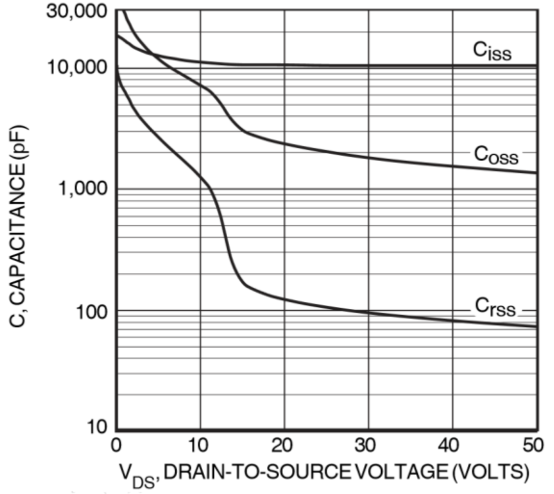
Exciter

Nearly total elimination of distortion at 25% modulation (Distortion approx. 0.05%)

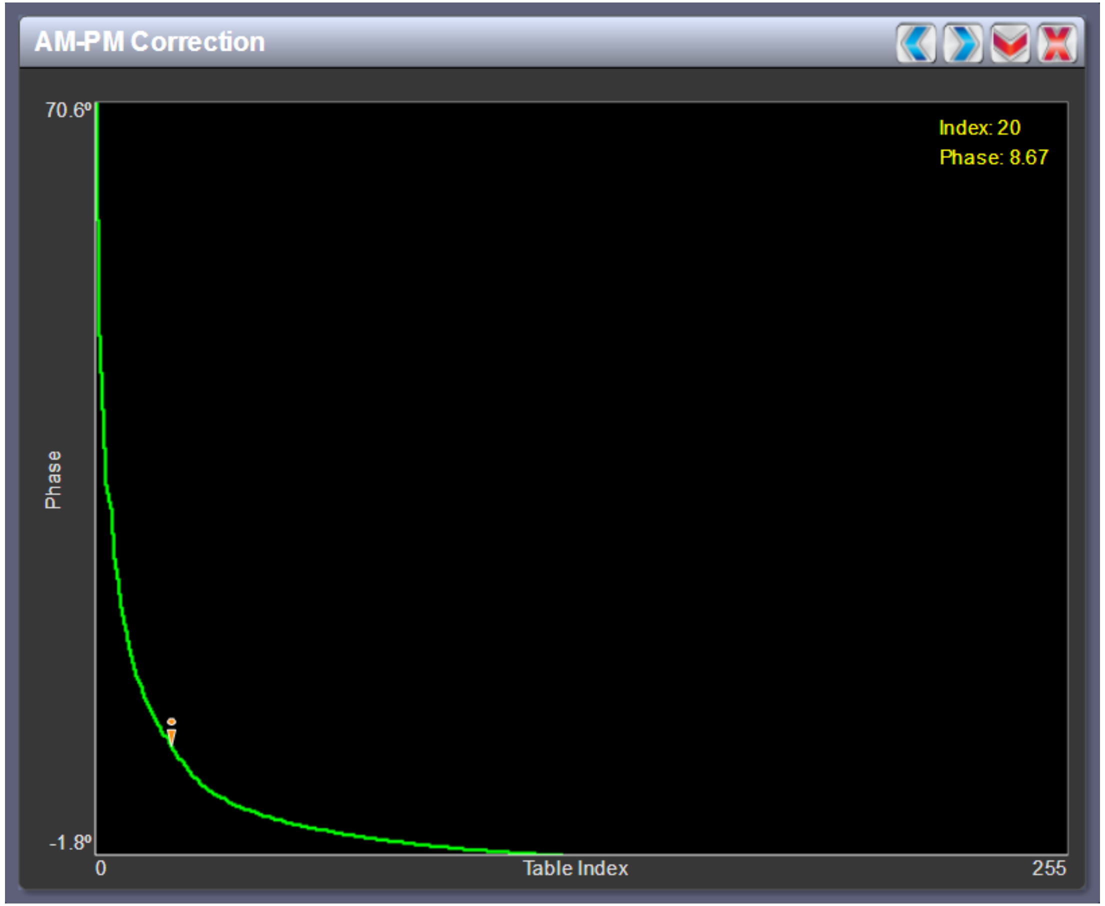


Exciter

AUI Screen
PM-AM
Correction



CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE



Power Supply

The AC power from the grid must be rectified so that it can be switched at the desired carrier frequency. AC/DC power conversions has two design possibilities:

- 50/60Hz rectification ‘big iron’
- Switching power supplies

In a nutshell the ‘big iron’ is very reliable and has excellent $/W at high power (>10kW)

Switching power supplies offer higher power density (W/in^3) , lower weight and higher redundancy

Power Supply

Regulations regarding the AM noise on the output RF signal would force the low pass filter following the rectifiers to be excessive.

Nautel patented a ‘lines volt compensation’ technique early on in its solid state designs that is continued to be used today.

Power Supply

Power supply design greatly affects the performance of the transmitter within the user's environment.

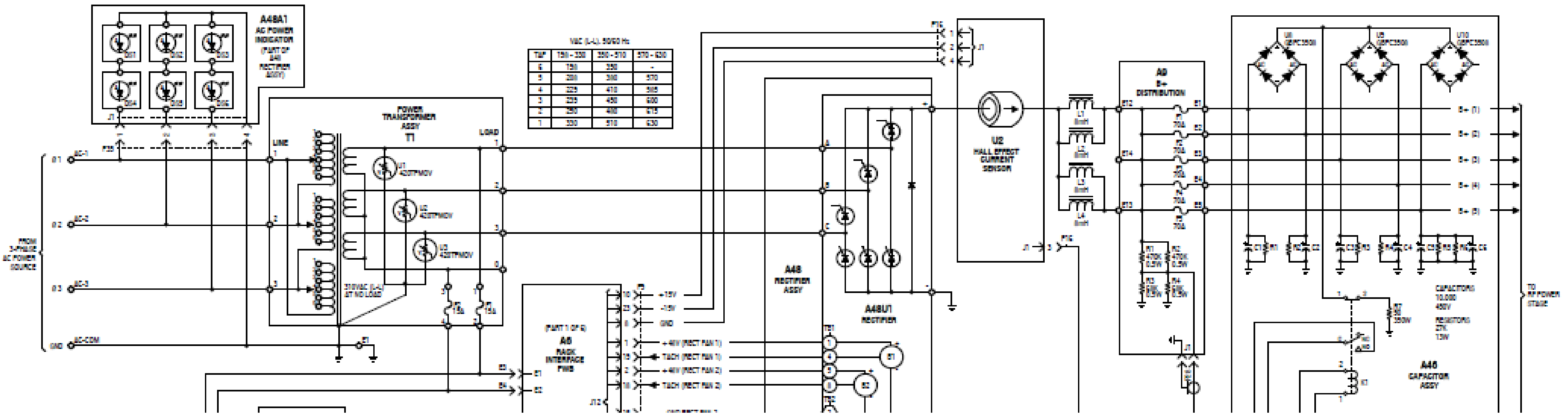
Big iron power supplies typically use SCR's for soft start and regulation but have power factor levels at approx. 0.93.

Power Supply

When running from generator, the transmitter's regulation circuits can make the load appear as a negative resistance causing instability in the generator's operation.

Also high power rectifiers can cause 'line notching' which drastically reduces the available power from the generator.

Power Supply



Circuit Board Design

Circuit board creation represents a significant portion of the total transmitter design effort.

Circuit boards typically use copper cladded epoxy resin (FR-4) but sometimes employ high quality materials (ie. Teflon) depending on the application.

FR-4 can operate at approx. 90C before discolouration and delamination.

The copper cladding is quantified in ‘ounces’ with each ounce resulting in 0.0014” thk of copper cladding.

Circuit Board Design

Nautel has strict guidelines for the current that a PWB conductor may carry versus the ounces of copper.

In high voltage applications, there are rules on creepage and clearance distances that must be followed for maximum reliability.

Nautel has an internal 100 point checklist that every PWB must pass before being manufactured.

Cooling

Transmitters employs multiple parallel DC cooling fans which provide:

- redundancy
- high efficiency
- not sync'd to AC line frequency

Protection

Transmitter's control function provides protection such as:

- SWR protection techniques (cutback, foldback, shutback)
- Thermal protection – fan tach, heatsink monitor
- Over current protection
- Over modulation protection

Thank You