

SERVICE INSTRUCTION

NAPC19

FIVE-LEVEL POWER TRIM ASSEMBLY



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INTRODUCTION

1. The NAPC19 five-level power trim assembly, when used in conjunction with an NAPE27 modulator driver module, provides the following control functions for its associated transmitter:

- (a) Provision to select one of five preset output power levels, locally or remotely.
- (b) Manual trim of output power level locally or remotely, provides up to a ten percent increase or a nine percent decrease from the preset output power level in one percent increments.

The NAPC19 five-level power trim assembly provides an alarm signal that indicates the power trim control circuit is at either its maximum or minimum position. It also provides outputs to indicate 'low level 1', 'low level 2', 'low level 3' or 'low level 4' has been selected. Troubleshooting and repair of the assembly is performed on a work bench independent of the associated transmitter. This document provides information necessary for a technician to understand the operation of the electrical circuits and the procedures to restore defective assemblies to a serviceable status, using tools and test equipment normally available at an AM radio station workshop. An alternative to procedures provided in this document is to utilize NAUTEL's module exchange/repair service facilities.

2. This paragraph has been deleted.

MECHANICAL CONFIGURATION

3. The NAPC19 five-level power trim assembly utilizes a formed metal box as its chassis. Electrical connection to the associated transmitter's driver unit is by mating two mass termination assembly (MTA) connectors on a flying lead, from the driver unit, to MTA square post headers (A1J1 and A1J2) on the assemblies printed circuit board A1. Electrical interconnection between the NAPC19 five-level power trim assembly and its associated NAPE27 modulator driver module is by an interconnecting cable that connects to locking, miniature, hexagonal connectors on their front panels. Controls and indicators are mounted on, or accessible through the front panel of the assembly. All electrical components, except the controls and indicators on the front panel, are mounted on a printed circuit board. The NAPC19 five-level power trim assembly is secured to the associated transmitter's driver unit by two screws that pass through two holes in its base plate. Refer to figure FO-4 for assembly detail of the NAPC19 five-level power trim assembly.

NAPC19 FIVE-LEVEL POWER TRIM ASSEMBLY OVERVIEW (see figure FO-1)

4. Figure FO-1 presents a block diagram of the NAPC19 five-level power trim assembly. The following overview description is based on this illustration. For a more detailed description refer to paragraph 5.

4.1 POWER LEVEL SELECTOR OVERVIEW: The power level selector circuit is a control/logic circuit that interfaces the local and remote power level selectors with the circuits that determine the associated transmitter's output power level. When the associated transmitter is operating in high power, the power level selector circuit will have no influence.

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4.1.1 Remote Low Power Control: With the associated transmitter set to REMOTE and LOW LEVEL SELECT switch S1 set to the RMT position, the low level control signals, including the low power control signal, are generated by the external 'low pwr' inputs at A1J1. Momentarily grounding one of the 'low pwr' inputs being applied to the power level selector circuit will produce a 'low power' control signal and also select the appropriate carrier level attenuator. The function of the 'low power' control signal is to set the associated transmitter's remote high/low relay to low and provide a 'reduce power' input signal to the power level selector circuit. Resetting the associated transmitter to high will inhibit the output of the power level selector circuit.

4.1.2 Local Low Power Control: With the associated transmitter set to LOCAL and LOW LEVEL SELECT switch S1 set to one of four low level positions, control signals from the power level selector latching relays will be inhibited. One of the four low level control signals selected by LOW LEVEL SELECT switch S1 will provide the selection of the appropriate carrier level attenuator and also one of four 'low level' status outputs for external use.

4.2 MODULATION BALANCE CONTROL OVERVIEW: The modulation balance control circuit provides the reference voltage used in the carrier level and power trim attenuator circuits. A potentiometer located in the modulation balance control circuit is set to provide a reference voltage at a level required to maintain a constant modulation 'depth' at all output power levels.

4.3 POWER TRIM CONTROL OVERVIEW: The power trim control circuit provides the clock, preset and up/down inputs to up/down counter A1U13 in the power trim attenuator circuit. With the Power Trim Source switch S3 set to REMOTE, a 'remote increase' control signal will provide a one hertz clock and a down command to the power trim attenuator circuit. A 'remote decrease' control signal will provide a one hertz clock and a up command to the power trim attenuator circuit. With the Power Trim Source switch S3 set to PRESET, the power trim attenuator circuit will be set to its preset position.

NOTE

When the +15 volt dc is first applied to the 'power trim control circuit, a momentary preset signal will be produced. With the Power Trim Source switch set to LOCAL, the one hertz clock command to the power trim attenuator circuit is controlled by the Power Trim switch S2.

4.4 POWER TRIM ATTENUATOR OVERVIEW: The power trim attenuator circuit provides a plus ten to minus nine percent variation in the associated transmitter's output power. This is achieved by the attenuating the 'carrier reference' signal, from the associated Nape27 modulation driver module, by a digitally controlled attenuator network. Up/down counter A1U13 of the power trim attenuator is controlled by the clock, preset and up/down input control signals from the power trim control circuit.

4.5 CARRIER LEVEL ATTENUATOR OVERVIEW: The carrier level attenuator circuit selects one of four variable resistors through the switching function of LOW LEVEL SELECT switch S1. The variable resistors in the carrier level attenuator circuit are preset to provide the required 'low level 1, 2, 3 or 4' outputs by attenuating the carrier control signal to the reference voltage established by the modulation control circuit.

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DETAILED THEORY OF OPERATION (see figures FO-2 and FO-3)

5. The following description expands on the overview presented in paragraph 4 and provides a detailed description of each function in the NAPC19 five-level power trim assembly, based on the electrical schematic depicted in figures FO-2 and FO-3.

5.1 POWER LEVEL SELECTOR DESCRIPTION: The power level selector circuit is a control/logic circuit that determines the source of low power level commands (local or remote) and generates the appropriate low power level control signals when the associated transmitter is not set to its high power level. When the associated transmitter is set to high power, the power level selector circuit will have no influence.

5.1.1 Remote Low Power Control: When an external ground potential 'low pwr 1, 2, 3 or 4' signal is applied to A1J1-1, 2, 3 or 4, a ground potential will be applied to A1J2-8 as the 'low power' output; a ground potential will also be applied to relays A1K1 and A1K2 resulting in the relays latching to their appropriate set/reset positions.

5.1.1.1 When a ground potential 'low pwr 1' command is applied to A1J1-1, this ground will be passed through diode A1CR5 to A1K1-5, the set coil of latching relay A1K1, and through diode A1CR9 to A1K2-5 and the set coil of latching relay A1K2. Relays A1K1 and A1K2 will latch to their set positions.

5.1.1.2 When a ground potential 'low pwr 2' command is applied to A1J1-2, this ground will be passed through diode A1CR6 to A1K1-5, the set coil of latching relay A1K1, and through diode A1CR11 to A1K2-1 and the reset coil of latching relay A1K2. Relay A1K1 will latch to its set position and relay A1K2 will latch to its reset position.

5.1.1.3 When a ground potential 'low pwr 3' command is applied to A1J1-3, this ground will be passed through diode A1CR7 to A1K1-1, the reset coil of latching relay A1K1, and through diode A1CR10 to A1K2-5 and the set coil of latching relay A1K2. Relay A1K1 will latch to its reset position and relay A1K2 will latch to its set position.

5.1.1.4 When a ground potential 'low pwr 4' command is applied to A1J1-4, this ground will be passed through diode A1CR8 to A1K1-1, the reset coil of latching relay A1K1, and through diode A1CR12 to A1K2-1 and the reset coil of latching relay A1K2. Relays A1K1 and A1K2 will latch to their reset positions.

5.1.2 Remote/Local Low Power Description: When the associated transmitter's high/low power control circuits are set to low power, a +15 volt dc (logic '1') 'reduce power' input will be applied to A1J1-11. A logic '1' level will be applied to the moving contacts of latching relays A1K1 and A1K2 as the input control logic for AND gates A1U1A, A1U1B, A1U1C or A1U1D. A 'reduced power' logic '1' level will also be applied simultaneously to one input of AND gates A1U3A, A1U3B, A1U3C and A1U3D. The section of AND gate A1U1 which has a logic '1' on both of its inputs will be determined by the set/reset status of latching relays A1K1/A1K2 (as described in paragraph 5.1.1). This gate will produce a logic '1' output while the remaining sections of AND gates A1U1 will produce a logic '0' output.

5.1.2.1 When LOW LEVEL SELECT switch S1 is set to 1, 2, 3 or 4, the transmitter's preset low power level will be locally determined by the setting of LOW LEVEL SELECT switch S1. A +15 volts dc (logic '1') will be applied to an input of A1U3A from S1-2, to A1U3B from S1-3, to A1U3C from S1-4 or to A1U3D from S1-5. The section of AND gate A1U3 which has a logic '1' (high) applied to both of its inputs will generate a logic '1' to one input of its respective OR gate (A1U4A/B/C or D). The logic '1' output of the active OR gate will be passed to the carrier level attenuator circuit as a 'LL1/LL2/LL3 or LL4' control signal. The logic '1' at the output of the active OR gate will also be applied through its respective inverter (A1U5D/E/F or G) to A1J2-1, 2, 3 or 5 representing a 'low level 1, 2, 3 or 4' control signal for external use.

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5.1.2.2 When LOW LEVEL SELECT switch S1 is set to RMT, +15 volts dc (logic '1') will be applied to one input of AND gates A1U2A, A1U2B, A1U2C and A1U2D from S1-1. The transmitter's preset low power level will be remotely determined by the output status of AND gates A1U1A, A1U1B, A1U1C and A1U1D (see paragraph 5.1.2). The section of AND gate A1U3 which has a logic '1' (high) applied to both of its inputs will generate a logic '1' to one input of its respective OR gate (A1U4A/B/C or D). The logic '1' output of the active OR gate will be passed to the carrier level attenuator circuit as a 'LL1/LL2/LL3 or LL4' control signal. The logic '1' at the output of the active OR gate will also be applied through its respective inverter (A1U5D/E/F or G) to A1J2-1, 2, 3 or 5 representing a 'low level 1, 2, 3 or 4' control signal for external use.

5.2 MODULATION BALANCE CONTROL DESCRIPTION: The modulation balance control circuit is comprised of MOD BAL potentiometer A1R12 and operational amplifier A1U6A. To maintain a constant modulation 'depth' for all four power levels, the attenuation of the 'carrier reference' input at J1-B must be to a voltage that corresponds to zero carrier output. This is achieved by establishing the MOD BAL reference at the output of A1U6A-1. MOD BAL potentiometer A1R12 is adjusted as per procedures outlined in the associated transmitter's alignment procedures to give a deflection between one-eighth and one-quarter inch (this deflection corresponds to approximately 1/1000th of the nominal rated output of the transmitter).

5.3 POWER TRIM CONTROL DESCRIPTION: The power trim control circuit consists primarily of one-second clock A1U12 and its associated components. The power trim control circuit provides local or remote control of the clock, and up/down inputs to the power trim attenuator circuit. Power Trim Source switch S3 when set to PRESET also generates a control input to the power trim control circuit for the purpose of setting up the associated transmitter's output power levels.

5.3.1 Power Trim Control-Remote/Local/Preset Description: Power Trim Source switch S3 provides a selection for either a remote or local 'increase/decrease' control signal for the power trim control circuit. It also provides a PRESET function for alignment procedures for the associated transmitter (see associated transmitter alignment procedures).

5.3.2 Preset Power Trim Control Description: When Power Trim Source switch S3 is set to PRESET, A1U10-2 will be at ground potential (logic '0'). The output at A1U10-3, which is applied to the 'PE' input of the up/down counter A1U13 in the power trim attenuator circuit, will be a logic '1' level. Up/down counter A1U13 will be set to an eight count (nominal setting).

5.3.3 Remote Power Trim Control Description: When the Power Trim Source switch S3 is set to REMOTE, an external 'remote increase' (logic '0') at A1J1-10 or 'remote decrease' (logic '0') at A1J1-9 is applied to inverters A1U8A or A1U8D.

5.3.3.1 When a 'remote increase' (logic '0') at A1J1-10 is applied to A1U7B, the resultant output at A1U7B-4 will be a logic '1'. When the two inputs to A1U8D are a logic '1', the output of A1U8B, which is applied to pin 6 of NOR gate A1U9B, will be a logic '1' level. A logic '0' output at pin 4 of A1U9B will be applied through diode A1CR17 to the 'MR' input of clock devise A1U12 while simultaneously a logic '0' will be applied from A1U7C-10 to the up/down input of A1U13.

5.3.3.2 When a 'remote decrease' (logic '0') at A1J1-9 is applied to A1U7A, the resultant output at A1U7A-3 will be a logic '1'. When the two inputs to A1U8A are a logic '1', the output of A1U8A, which is applied to pin 1 of NOR gate A1U9A, will be a logic '1' level. A logic '0' output at pin 3 of A1U9A will be applied through diode A1CR18 to the 'MR' input of clock devise A1U12 while simultaneously a logic '1' will be applied from A1U7C-10 to the up/down input of A1U13.

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5.3.4 Local Power Trim Control Description: When the Power Trim Source switch S3 is set to LOCAL, the INCREASE (logic '1') at A1-J or 'DECREASE' (logic '1') at A1-K is controlled by spring loaded Power Trim switch S2. The resultant logic output from switch S2 (INCREASE or DECREASE) will be applied to the input of either A1U8B-5 or A1U8C-8.

5.3.4.1 When spring loaded Power Trim switch S2 is set to INCREASE, a +15 volt dc (logic '1') at A1-K is applied to A1U8C-8. When the two inputs to A1U8C are a logic '1', the output of A1U8C, which is applied to pin 5 of NOR gate A1U9B, will be a logic '1' level. A logic '0' output at pin 4 of A1U9B will be applied through diode A1CR17 to the 'MR' input of clock device A1U12 while simultaneously a logic '0' will be applied from A1U7C-10 to the up/down input of A1U13.

5.3.4.2 When spring loaded Power Trim switch S2 is set to DECREASE, a +15 volt dc (logic '1') at A1-J is applied to A1U8B-5. When the two inputs to A1U8B are a logic '1', the output of A1U8B, which is applied to pin 2 of NOR gate A1U9A, will be a logic '1' level. A logic '0' output at pin 3 of A1U9A will be applied through diode A1CR18 to the A1U13-MR input of clock device A1U12 while simultaneously a logic '1' will be applied from A1U7C-10 to the up/down input of A1U13.

5.3.5 Power Trim Control Clock Description: When the input to A1U12-MR is a logic '0' (active state), the 1 Hz clock reset control output at A1U12-Q will be applied to A1U12-6. When the input to A1U12-MR is a logic '1' (inactive state), the 1 Hz clock reset control output at A1U12-Q will be inhibited.

5.4 POWER TRIM ATTENUATOR DESCRIPTION: The power trim attenuator consists of up/down counter A1U13, analog switches A1U11A thru A1U11-D and their associated components. Attenuation of the 'carrier reference' input is performed with the associated transmitter being controlled from a local or remote location. The power trim attenuator allows a variation of plus ten percent to minus nine percent relative to the PRESET level. Attenuation is done in a binary function with the smallest of each of the 16 steps representing approximately one percent in output power.

5.4.1 Preset-Power Trim Attenuator Description: When Power Trim Source switch S3 is set to PRESET, a ground potential (logic '0') is applied from the power trim control circuit to A1U13-PE, a zero reference voltage at A1U13-PE sets up/down counter A1U13 at the nominal range by generating a selected binary output to analog switch A1U11-D. A1U11-D will turn on and the 'carrier reference' input at J1-A will be attenuated through resistor A1R24 and A1R28.

5.4.2 Increase-Power Trim Attenuator Description: A logic '0' input at A1U13-10 in conjunction with a 1 hertz clock input at A1U13-15 will cause up/down counter A1U13 to count down in one step increments. This down count will continue until the increase control is removed. Should the increase control remain low until the output of A1U13 reaches '0000', the carry out signal on A1U13-7 will inhibit the clock input via gate A1U10C, while providing a 'power trim alarm' output at A1J2-6 via A1U10B and A1U5C-14. The binary function of A1U13 will select the appropriate analog switch configuration through outputs at A1U13-Q0/Q1/Q2/Q3 and attenuate the 'carrier reference' input through A1R24 and the selected analog attenuator resistors A1R25 thru A1R28.

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5.4.3 Decrease-Power Trim Attenuator Description: A logic '1' input at A1U13-10 in conjunction with a 1 hertz clock input at A1U13-15 will cause up/down counter A1U13 to count up in one step increments. Should the counter reach a state of '1111', with the input to A1U13-10 high, the carry out signal at A1U13-7 will inhibit the 'clock' input at A1U13-15 and produce a 'power trim alarm' output at A1J2-6 via A1U10B and A1U5C-14. The binary function of A1U13 will select the appropriate analog switch configuration through outputs at A1U13-Q0/Q1/Q2/Q3 and attenuate the 'carrier reference' input at J1-A through A1R24 and selected analog attenuator resistors A1R25 thru A1R28.

5.5 CARRIER LEVEL ATTENUATOR DESCRIPTION: The 'carrier reference' signal from associated modulator driver module NAPE27, is passed through J1-A and buffered by A1U6B, the signal is then applied through resistor A1R24 and attenuated by an amount determined by the up/down counter A1U13. The 'carrier reference' input signal is then buffered by A1U6C and attenuated through the function of a low level attenuator network comprising A1R29 and low level O/PS potentiometers, A1R31, A1R33, A1R35 or A1R37. The low level o/ps attenuator circuit is controlled by the 'LL1', 'LL2', 'LL3' or 'LL4' inputs from the power level selector circuit.

5.5.1 LOW LEVEL O/PS-1 potentiometer A1R31 in conjunction with power MOSFET A1Q1 allows adjustment of the transmitter's 'low pwr 1' rf output level; LOW LEVEL O/PS-2 potentiometer A1R33 in conjunction with power MOSFET A1Q2 allows adjustment of the transmitter's 'low pwr 2' rf output level; LOW LEVEL O/PS-3 potentiometer A1R35 in conjunction with power MOSFET A1Q3 allows adjustment of the transmitter's 'low pwr 3' rf output level and LOW LEVEL O/PS-4 potentiometer A1R37 in conjunction with power MOSFET A1Q4 allows adjustment of the transmitter's 'low pwr 4' rf output level. When the transmitter is in the high power state, no attenuation occurs across A1R29. The signal is then buffered by A1U6D and applied through J1-B to the NAPE27 modulator driver module as a pulse-width modulator control signal.

NOTE

The low level potentiometers allow the low level outputs to be set between zero percent and eighty percent of the high output level. Where it is necessary to have a low level greater than eighty percent of the high output, the values of A1R29 and/or the associated LOW LEVEL O/PS potentiometers may be changed.

TROUBLESHOOTING

6. Troubleshooting NAPC19 five-level power trim assemblies that are defective, or suspect of being defective, consists of performing a visual inspection and then conducting a functional test to isolate the defective components.

6.1 TEST EQUIPMENT AND SPECIAL TOOLS: The test equipment required is listed in table 1. There are no special tools required.

6.2 REMOVAL OF NAPC19 FIVE-LEVEL POWER TRIM ASSEMBLY: To remove the NAPC19 five-level power trim assembly from a transmitter for visual inspection and testing, it is necessary to remove the mounting screws fastening it to the driver unit assembly. These screws are accessible by removing the modulator module directly below the NAPC19, or in the case of an AMPFET 1 transmitter, by removing the control panel.

NOTE

Follow normal safety procedures before removing the appropriate unit.
Refer to associated transmitter's technical instruction manual.

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6.3 **VISUAL INSPECTION:** It is recommended that a visual inspection be performed on the NAPC19 five-level power trim assembly before conducting electrical tests. Inspect for the following:

- (a) Inspect all electrical components for evidence of overheating or physical damage.
- (b) Inspect all solder connections for good mechanical bond and adequate solder.
- (c) Verify that no wiring insulation is damaged.
- (d) Verify that wire strands of wiring conductors are not broken or otherwise damaged.
- (e) Verify the chassis and printed circuit board is free from solder slivers and other conductive foreign objects.
- (f) Verify all integrated circuit devices are installed and firmly seated in their sockets.
- (g) Verify all fastening hardware is securely tightened.

6.4 **FUNCTIONAL TEST:** Functional testing of the NAPC19 five-level power trim assembly is the recommended first step in troubleshooting a defective assembly. It also verifies the assembly is operating within design limits after corrective action has been taken. Assemblies that meet the requirements of the functional test may be considered to be operating satisfactorily and returned to service.

NOTE

Final adjustment of the NAPC19 five-level power trim assembly is performed with the assembly installed in its associated transmitter. In particular, it may be necessary to adjust MOD BAL potentiometer A1R12 after the assembly has been installed in the transmitter.

6.4.1 Preparation for Test: Prepare the NAPC19 five-level power trim assembly for test as follows:

- (a) Verify the visual inspection has been completed.
- (b) Connect the assembly to be tested to the test setup shown in figure 1.
- (c) Set NAPC19 assembly switches as follows:
 - (i) - Power Trim Source (S3) to PRESET
 - (ii) - Power Trim (S2) to OFF
 - (iii) - LOW LEVEL SELECT (S1) to RMT
- (d) Connect digital multimeter to A1U6A-1 (+) and chassis ground (-).
- (e) Measure and record dc voltage indication on digital multimeter mentioned in step (d).

6.4.2 Modulation Balance Control Test: Check the modulation balance control function as follows:

- (a) Adjust the MOD BAL potentiometer A1R12 fully clockwise.
- (b) Simultaneously monitor the indication at A1U6A-1 while slowly adjusting MOD BAL potentiometer A1R12 fully counterclockwise.

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- (c) Digital multimeter indication in step (b) shall be a smooth transition from 5.5 volts dc to 9.5 volts dc.
- (d) Set MOD BAL potentiometer A1R12 for a 7.5 volts dc indication on digital multimeter at A1U6A-1.
- (e) Remove digital multimeter from A1U6-1 and reconnect multimeter to 'PWM control' at J1-B.
- (f) Adjust R1 of the test setup to give 6.0 volts dc indication on digital multimeter connected at J1-B.

6.4.3 Power Trim Test: Check the remote/local operation of the power trim function as follows:

- (a) Connect digital multimeter between A1J2-6 (+) and chassis ground (-).
- (b) Digital multimeter indication shall be a nominal +15 volts dc.
- (c) Set Power Trim Source switch S3 to REMOTE.
- (d) Connect digital multimeter between J1-B (+) and chassis ground (-).
- (e) Record digital multimeter indication (should be 6.0 volts dc).
- (f) Simultaneously monitor digital multimeter indication and connect a ground to A1J1-10.
- (g) Digital multimeter indication shall decrease in eight 0.01 volt steps and remain constant at 5.92 volts dc. [0.08 volts dc less than voltage recorded in step (e)].
- (h) Connect digital multimeter between A1J2-6 (+) and chassis ground (-).
- (i) Digital multimeter indication shall be a nominal zero volts.
- (j) Connect digital multimeter between J1-B (+) and chassis ground (-).
- (k) Remove ground, connected in step (f), from A1J1-10 and note digital voltmeter indication at J1-B remains constant at 5.92 volts dc.
- (l) Simultaneously monitor digital multimeter indication and connect a ground to A1J1-9.
- (m) Digital multimeter indication shall increase in fifteen 0.01 volt steps and remain constant at 6.07 volts dc. [0.07 volts dc more than voltage recorded in step (e)].
- (n) Connect digital multimeter between A1J2-6 (+) and chassis ground (-).
- (o) Digital multimeter indication shall be a nominal zero volts.
- (p) Connect digital multimeter between J1-B (+) and chassis ground (-).
- (q) Remove ground, connected in step (l), from A1J1-9 and note digital voltmeter indication at J1-B remains constant at 6.07 volts dc.

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- (r) Set Power Trim Source switch S3 to PRESET.
- (s) Digital multimeter indication shall go to the voltage recorded in step (e) (6.0 volts dc).
- (t) Set Power Trim Source switch S3 to LOCAL.
- (u) Simultaneously monitor digital multimeter indication and hold Power Trim switch S2 in its spring-loaded INCREASE position (S2-5).
- (v) Digital multimeter indication shall decrease in 0.01 volt steps and remain constant at 5.92 volts dc after the eighth step (0.08 volts dc less than voltage recorded in step (e)).
- (w) Release Power Trim switch S2 and note digital voltmeter indication remains constant at 5.92 volts dc.
- (x) Simultaneously monitor digital multimeter indication and hold Power Trim switch S2 in its spring-loaded DECREASE position (S2-1).
- (y) Digital multimeter indication shall increase in 0.01 volt steps and remain constant at 6.07 volts dc after the fifteenth step (0.07 volts dc more than voltage recorded in step (e)).
- (z) Release Power Trim switch S2 and note digital voltmeter indication remains constant at 6.07 volts dc.
- (aa) Disconnect digital multimeter from J1-B.

6.4.4 Local 'Low Level 1' Test: Check the local 'low level 1' function as follows:

- (a) Verify the NAPC19 five-level power trim assembly is connected as detailed in paragraph 6.4.1.
- (b) Connect the +15 volt dc power supply between A1J1-11 (+) and chassis ground (-).
- (c) Set LOW LEVEL SELECT switch S1 to position '1' (this corresponds to local selection of 'low level 1').
- (d) Record the voltage indication on digital multimeter connected at J1-B.
- (e) Simultaneously monitor the voltage indication on digital multimeter connected at J1-B while slowly adjusting LOW LEVEL O/PS-1 potentiometer A1R31 fully clockwise.
- (f) Digital multimeter indication in step (e) shall be a maximum of 6.2 volts dc.
- (g) Simultaneously monitor the voltage indication at J1-B while slowly adjusting LOW LEVEL O/PS-1 potentiometer A1R31 fully counterclockwise.
- (h) Digital multimeter indication mentioned in step (g) shall be a minimum of 7.4 volts dc.
- (i) Monitor digital multimeter connected at J1-B and set LOW LEVEL O/PS-1 potentiometer A1R31 for an indication that was previously recorded in step (d).

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6.4.5 Local 'Low Level 2' Test: Check the local 'low level 2' function as follows:

- (a) Set LOW LEVEL SELECT switch S1 to position '2' (this corresponds to local selection of 'low level 2').
- (b) Repeat steps 6.4.4(d) thru 6.4.4(i), adjusting LOW LEVEL O/PS-2 potentiometer A1R33 rather than A1R31 potentiometer.

6.4.6 Local 'Low Level 3' Test: Check the local 'low level 3' function as follows:

- (a) Set LOW LEVEL SELECT switch S1 to position '3' (this corresponds to local selection of 'low level 3').
- (b) Repeat steps 6.4.4(d) thru 6.4.4(i), adjusting LOW LEVEL O/PS-3 potentiometer A1R35 rather than A1R31 potentiometer.

6.4.7 Local 'Low Level 4' Test: Check the local 'low level 4' function as follows:

- (a) Set LOW LEVEL SELECT switch S1 to position '4' (this corresponds to local selection of 'low level 4').
- (b) Repeat steps 6.4.4(d) thru 6.4.4(i), adjusting LOW LEVEL O/PS-4 potentiometer A1R37 rather than A1R31 potentiometer.

6.4.8 Remote Low Level Test: Check the remote low level functions as follows:

- (a) Set LOW LEVEL SELECT switch S1 to RMT.
- (b) Remove the +15 volt dc power supply from A1J1-11 and reconnect power supply as shown for test setup in figure '1'.
- (c) Digital multimeter indication at J1-B will be 6.0 volts dc (corresponding to high carrier level).
- (d) Disconnect digital multimeter from J1-B.
- (e) Connect positive lead of digital multimeter to A1J2-1, A1J2-2, A1J2-3 and A1J2-5 respectively and chassis ground (-).
- (f) Digital multimeter indications will be a nominal +15 volts dc for each reading obtained in step (e).
- (g) Connect the +15 volt dc power supply between A1J1-11 (+) and chassis ground (-).
- (h) Connect digital multimeter between J1-B (+) and chassis ground (-).
- (i) Momentarily apply a ground to 'low pwr 1' input at A1J1-1.
- (j) Digital multimeter indication on J1-B should be that recorded in paragraph 6.4.4(d) (corresponding to 'low level 1').
- (k) Disconnect digital multimeter from J1-B and connect multimeter between A1J2-1 (+) and chassis ground (-).

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- (l) Digital multimeter indication at A1J2-1 shall be zero volts.
- (m) Disconnect digital multimeter from A1J2-1 and connect multimeter between J1-B (+) and chassis ground (-).
- (n) Momentarily apply a ground to 'low pwr 2' input at A1J1-2.
- (o) Digital multimeter indication on J1-B should be that recorded in paragraph 6.4.5(d) (corresponding to 'low level 2').
- (p) Disconnect digital multimeter from J1-B and connect multimeter between A1J2-2 (+) and chassis ground (-).
- (q) Digital multimeter indication at A1J2-2 shall be zero volts.
- (r) Disconnect digital multimeter from A1J2-2 and connect multimeter between J1-B (+) and chassis ground (-).
- (s) Momentarily apply a ground to 'low pwr 3' input at A1J1-3.
- (t) Digital multimeter indication on J1-B should be that recorded in paragraph 6.4.6(d) (corresponding to 'low level 3').
- (u) Disconnect digital multimeter from J1-B and connect multimeter between A1J2-3 (+) and chassis ground (-).
- (v) Digital multimeter indication at A1J2-3 shall be zero volts.
- (w) Disconnect digital multimeter from A1J2-3 and connect multimeter between J1-B (+) and chassis ground (-).
- (x) Momentarily apply a ground to 'low pwr 4' input at A1J1-4.
- (y) Digital multimeter indication on J1-B should be that recorded in paragraph 6.4.7(d) (corresponding to 'low level 4').
- (z) Disconnect digital multimeter from J1-B and connect multimeter between A1J2-5 (+) and chassis ground (-).
- (aa) Digital multimeter indication at A1J2-5 shall be zero volts.

6.5 COMPLETION OF TESTS: NAPC19 five-level power trim assemblies that meet all requirements of paragraph 6.4 and may be considered to be satisfactory and returned to service. Upon installation in the transmitter, it may be necessary to realign assembly controls to meet the operational requirements of the transmitter. Refer to the installation and calibration procedures of the associated transmitter's technical instruction manual.

6.6 INSERVICE ALIGNMENT OF MOD BAL: Due to variations within individual transmitters, it may be necessary to realign MOD BAL potentiometer A1R12 after the assembly has been installed.

- (a) Switch on transmitter and set LOW LEVEL SELECT switch S1 to position '3' (low level 2).

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- (b) Adjust LOW LEVEL O/PS potentiometer A1R33 fully counterclockwise for a minimum output power.
- (c) The indicated output power should give a deflection of between one-quarter and one-eighth inch on the forward power meter in its lowest range. If this is the case, no adjustment of MOD BAL potentiometer A1R12 is necessary.
- (d) Should the deflection on the FWD PWR meter be greater than one-quarter inch, adjust MOD BAL potentiometer A1R12 until a deflection between one-eighth and one-quarter inch is achieved.
- (e) Should the MOD DRIVE alarm turn on, adjust MOD BAL potentiometer A1R12 by one-quarter turn and reset the transmitter, if necessary.
- (f) Repeat steps (c) thru (e) until a deflection of one-eighth to one-quarter inch is achieved with no mod drive alarm.
- (g) The transmitter should now be ready for normal operation. However, it may be necessary to readjust output level controls following realignment of MOD BAL potentiometer A1R12.

REPAIR

7. There are no special repair procedures for the NAPC five-level power trim assembly other than normal precautions to be observed when handling CMOS devices. Gain access to the printed wiring side of printed circuit board A1 by removing four countersunk screws on the outside of the chassis and swinging the printed circuit board on its cable harness without removing the interconnecting wires. Upon reassembly, ensure wires are not pinched when the screws are tightened.

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Table 1 Test Equipment

NOMENCLATURE	PART, MODEL, OR TYPE NUMBER (EQUIVALENTS MAY BE USED)
Digital Multimeter	3 1/2 digit, ac and dc volts ohms and amps, ±0.5% accuracy, Beckman 3010
Oscilloscope	15 MHz Tektronix Model T922
15 Vdc Power Supply	15 volts dc, 1 ampere
24 Vdc Power Supply	24 volts dc, 1 ampere
Resistor	7 - 1000 ohms
Potentiometer	1 - 1000 ohms
Clip leads	

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Table 2 Wiring List - NAPC19 Five-Level Power Trim Assembly

SOURCE	DESTINATION	CODE	SIZE	REMARKS
J1-A	A1-A	1 White	24	Twisted Pair Twisted Pair
J1-B	A1-B	2 White	24	
J1-D	A1-E	3 White	24	
J1-E	A1-D	4 White	24	
J1-F	A1-F	5 Red	24	
J1-H	A1-H	6 Black	24	
A1-J	S2-1	7 White	24	
A1-K	S2-5	8 White	24	
A1-L	S2-3	9 Red	24	
S2-3	S3-2	10 Red	24	
S3-2	S3-3	11 Red	24	
S3-3	S3-6	12 Red	24	
A1-M	S3-5	13 White	24	
A1-N	S3-1	14 White	24	
A1-P	S3-4	15 White	24	
S3-6	S1-1 C-W	16 Red	24	
A1-R	S1-1 C-1	17 White	24	
A1-S	S1-1 C-2	18 White	24	
A1-T	S1-1 C-3	19 White	24	
A1-U	S1-1 C-4	20 White	24	
A1-V	S1-1 C-5	21 White	24	

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Table 3 NAPC19 Reference Designation Index

REF DES	NAME OF PART AND DESCRIPTION	NAUTEL's PART NO.	JAN, MIL OR MFR PART NO.
-	Five-Level Power Trim Assembly	NAPC19	139-3140
A1	Five-Level Power Trim PCB Assembly	139-3144	139-3144
A1C1	Capacitor, Ceramic, 0.1uF 10%, 100V	CCG07	CKR06BX104KL
A1C2	Capacitor, Tantalum, 6.8uF 10%, 35V	CCP19	CSR13F685KM
A1C3	Capacitor, Ceramic, 0.1uF 10%, 100V	CCG07	CKR06BX104KL
A1C4	Capacitor, Ceramic, 0.001uF 10%, 200V	CCG01	CKR05BX102KL
A1C5	Capacitor, Ceramic, 0.001uF 10%, 200V	CCG01	CKR05BX102KL
A1C6	Capacitor, Ceramic, 0.01uF 10%, 100V	CCG04	CKR05BX103KL
A1C7	Capacitor, Mica, 1000pF 2%, 500V	CB37	CM06FD102G03
A1C8	Capacitor, Tantalum, 1.0uF 10%, 50V	CCP24	CSR13G105KM
A1C9	Capacitor, Ceramic, 0.01uF 10%, 100V	CCG04	CKR05BX103KL
A1CR1	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR2	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR3	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR4	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR5	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR6	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR7	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR8	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR9	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR10	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR11	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR12	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR13	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR14	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR15	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR16	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR17	Diode, General Purpose, Small Signal	QAP29	1N4938
A1CR18	Diode, General Purpose, Small Signal	QAP29	1N4938
A1J1	MTA, Square Post Header Assy, 12-pin	JU21	1-640383-2
A1J2	MTA, Square Post Header Assembly, 8-Pin	JU08	640383-8
A1K1	Relay, Latching, 24Vdc Coil	KB20	G2NK-2124P-DC24
A1K2	Relay, Latching, 24Vdc Coil	KB20	G2NK-2124P-DC24
A1Q1	Transistor, Field Effect, N Channel	QA36	IRFF112
A1Q2	Transistor, Field Effect, N Channel	QA36	IRFF112
A1Q3	Transistor, Field Effect, N Channel	QA36	IRFF112
A1Q4	Transistor, Field Effect, N Channel	QA36	IRFF112
A1R1	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R2	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R3	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R4	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R5	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R6	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R7	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R8	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R9	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R10	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G

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Table 3 NAPC19 Reference Designation Index

REF DES	NAME OF PART AND DESCRIPTION	NAUTEL's PART NO.	JAN, MIL OR MFR PART NO.
A1R11	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R12	Resistor, Variable, 10K ohms, 3/4W	RW32	43P103
A1R13	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R14	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R15	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R16	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R17	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R18	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R19	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R20	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R21	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R22	Resistor, Film, 5600 ohms, 2% 1/2W	RAP12	RL20S562G
A1R23	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R24	Resistor, Film, 680 ohms, 2% 1/2W	RC35	RL20S681G
A1R25	Resistor, Film, 100K ohms, 1% 1/2W	RP28	M22D-100K Ohms-1%
A1R26	Resistor, Film, 49.9K ohms, 1% 1/2W	RS32	RN60D4992F
A1R27	Resistor, Film, 24.9K ohms, 1% 1/2W	RS33	RN60D2492F
A1R28	Resistor, Film, 12.4K ohms, 1% 1/2W	RQ29	M22D-12.4K Ohms-1%
A1R29	Resistor, Film, 1000 ohms, 2% 1/2W	RAP09	RL20S102G
A1R30	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R31	Resistor, Variable, 10K ohms, 3/4W	RW32	43P103
A1R32	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R33	Resistor, Variable, 10K ohms, 3/4W	RW32	43P103
A1R34	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R35	Resistor, Variable, 10K ohms, 3/4W	RW32	43P103
A1R36	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R37	Resistor, Variable, 10K ohms, 3/4W	RW32	43P103
A1R38	Resistor, Film, 330 ohms, 2% 1/2W	RAP07	RL20S331G
A1R39	Resistor, Film, 5600 ohms, 2% 1/2W	RAP12	RL20S562G
A1U1	IC, CMOS, Quad, 2-input AND Gates	UB20	MC14081BAL
A1U2	IC, CMOS, Quad, 2-input AND Gates	UB20	MC14081BAL
A1U3	IC, CMOS, Quad, 2-input AND Gates	UB20	MC14081BAL
A1U4	IC, CMOS, Quad, 2-input OR Gates	UB22	MC14071BAL
A1U5	IC, Transistor Array, 7 Darlington's	UL15	ULN2004A
A1U6	IC, Operational Amplifiers, Quad	UC15	MC3403L
A1U7	IC, CMOS, Quad, 2-input NAND Gates	UB03	MC14011BAL
A1U8	IC, CMOS, Quad, 2-input AND Gates	UB20	MC14081BAL
A1U9	IC, CMOS, Quad, 2-input NOR Gates	UB01	MC14001BAL
A1U10	IC, CMOS, Quad, 2-input NAND Gates	UB03	MC14011BAL
A1U11	IC, CMOS, Quad, Analog Switch	UB10	MC14066BAL
A1U12	IC, CMOS, Oscillator/Timer	UB12	MC14541BAL
A1U13	IC, CMOS, Binary Up/Down Counter	UC10	MC14516BAL
A1XU1	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU2	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU3	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU4	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU5	Socket, Integrated Circuit, 16-pin	UC03	640358-1

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Table 3 NAPC19 Reference Designation Index

REF DES	NAME OF PART AND DESCRIPTION	NAUTEL's PART NO.	JAN, MIL OR MFR PART NO.
A1XU6	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU7	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU8	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU9	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU10	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU11	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU12	Socket, Integrated Circuit, 14-pin	UC02	640357-1
A1XU13	Socket, Integrated Circuit, 16-pin	UC03	640358-1
J1	Connector, 7-pin, Panel Mount	J001	126-198
S1	Switch, Rotary, Miniature, 2P5P	SCP02	MRB-2-5S
S2	Switch, Toggle Momentary 2PDT	SC20B	MST-205S
S3	Switch, Toggle, 2PDT, Centre Off	SA22B	MST-205P

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Table 4 NAPC19 Parts Per Unit Index

NAUTEL's PART NO.	NAME OF PART AND DESCRIPTION	JAN, MIL OR MFR PART NO.	OEM CODE	TOTAL IDENT PARTS
NAPC19	Five-Level Power Trim Assembly	139-3140	37338	-
139-3144	Five-Level Power Trim PCB Assembly	139-3144	37338	1
CB37	Capacitor, Mica, 1000pF 2%, 500V	CM06FD102G03	14655	1
CCG01	Capacitor, Ceramic, 0.001uF 10%, 200V	CKR05BX102KL	56289	2
CCG04	Capacitor, Ceramic, 0.01uF 10%, 100V	CKR05BX103KL	56289	2
CCG07	Capacitor, Ceramic, 0.1uF 10%, 100V	CKR06BX104KL	56289	2
CCP19	Capacitor, Tantalum, 6.8uF 10%, 35V	CSR13F685KM	56289	1
CCP24	Capacitor, Tantalum, 1.0uF 10%, 50V	CSR13G105KM	56289	1
J001	Connector, 7-pin, Panel Mount	126-198	02660	1
JU08	MTA, Square Post Header Assembly, 8-Pin	640383-8	09482	1
JU21	MTA, Square Post Header Assy, 12-pin	1-640383-2	09482	1
KB20	Relay, Latching, 24Vdc Coil	G2NK-2124P-DC24	34361	2
QA36	Transistor, Field Effect, N Channel	IRFF112	81483	4
QAP29	Diode, General Purpose, Small Signal	1N4938	01295	18
RAP07	Resistor, Film, 330 ohms, 2% 1/2W	RL20S331G	36002	1
RAP09	Resistor, Film, 1000 ohms, 2% 1/2W	RL20S102G	36002	1
RAP12	Resistor, Film, 5600 ohms, 2% 1/2W	RL20S562G	36002	2
RAP13	Resistor, Film, 10K ohms, 2% 1/2W	RL20S103G	36002	3
RAP17	Resistor, Film, 100K ohms, 2% 1/2W	RL20S104G	36002	22
RC35	Resistor, Film, 680 ohms, 2% 1/2W	RL20S681G	36002	1
RP28	Resistor, Film, 100K ohms, 1% 1/2W	M22D-100K Ohms-1%	36002	1
RQ29	Resistor, Film, 12.4K ohms, 1% 1/2W	M22D-12.4K Ohms-1%	36002	1
RS32	Resistor, Film, 49.9K ohms, 1% 1/2W	RN60D4992F	36002	1
RS33	Resistor, Film, 24.9K ohms, 1% 1/2W	RN60D2492F	36002	1
RW32	Resistor, Variable, 10K ohms, 3/4W	43P103	02111	5
SA22B	Switch, Toggle, 2PDT, Centre Off	MST-205P	95146	1
SC20B	Switch, Toggle Momentary 2PDT	MST-205S	95146	1
SCP02	Switch, Rotary, Miniature, 2P5P	MRB-2-5S	95146	1
UB01	IC, CMOS, Quad, 2-input NOR Gates	MC14001BAL	04713	1
UB03	IC, CMOS, Quad, 2-input NAND Gates	MC14011BAL	04713	2
UB10	IC, CMOS, Quad, Analog Switch	MC14066BAL	04713	1
UB12	IC, CMOS, Oscillator/Timer	MC14541BAL	04713	1
UB20	IC, CMOS, Quad, 2-input AND Gates	MC14081BAL	04713	4
UB22	IC, CMOS, Quad, 2-input OR Gates	MC14071BAL	04713	1
UC02	Socket, Integrated Circuit, 14-pin	640357-1	00779	11
UC03	Socket, Integrated Circuit, 16-pin	640358-1	00779	2
UC10	IC, CMOS, Binary Up/Down Counter	MC14516BAL	04713	1
UC15	IC, Operational Amplifiers, Quad	MC3403L	04713	2

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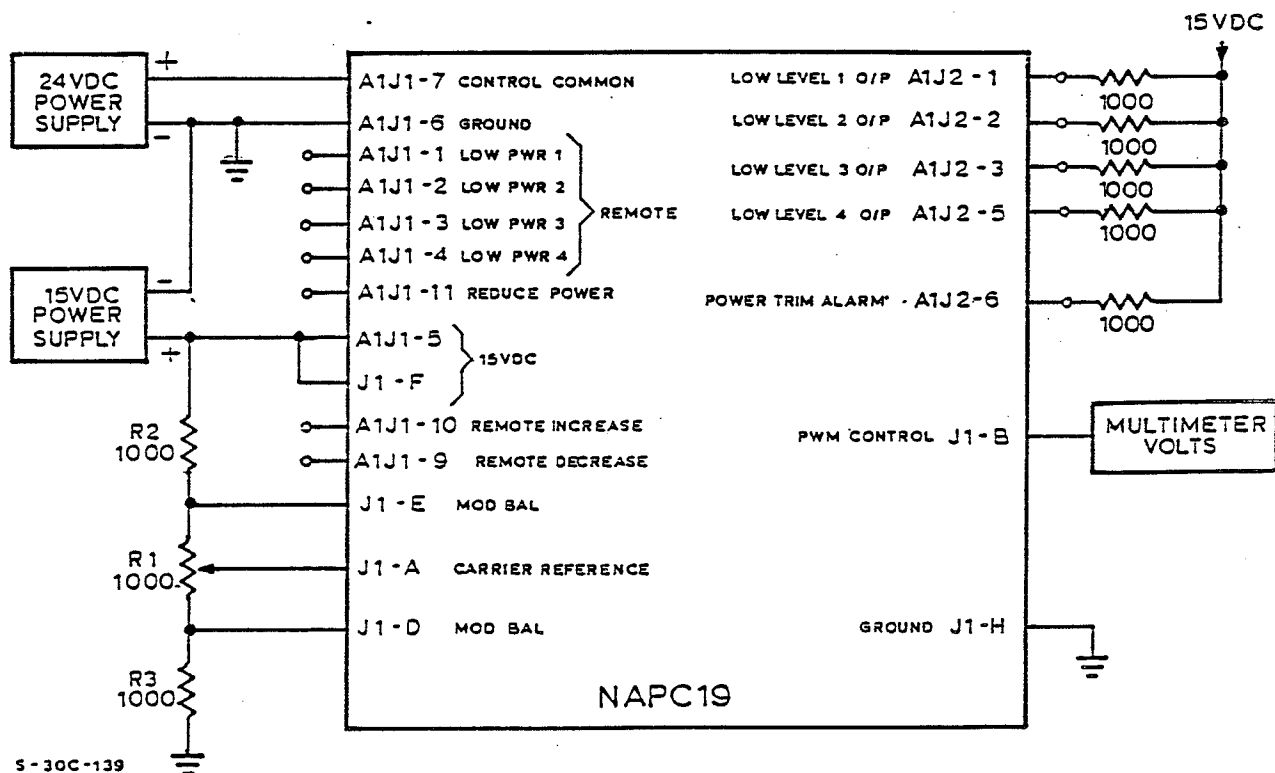
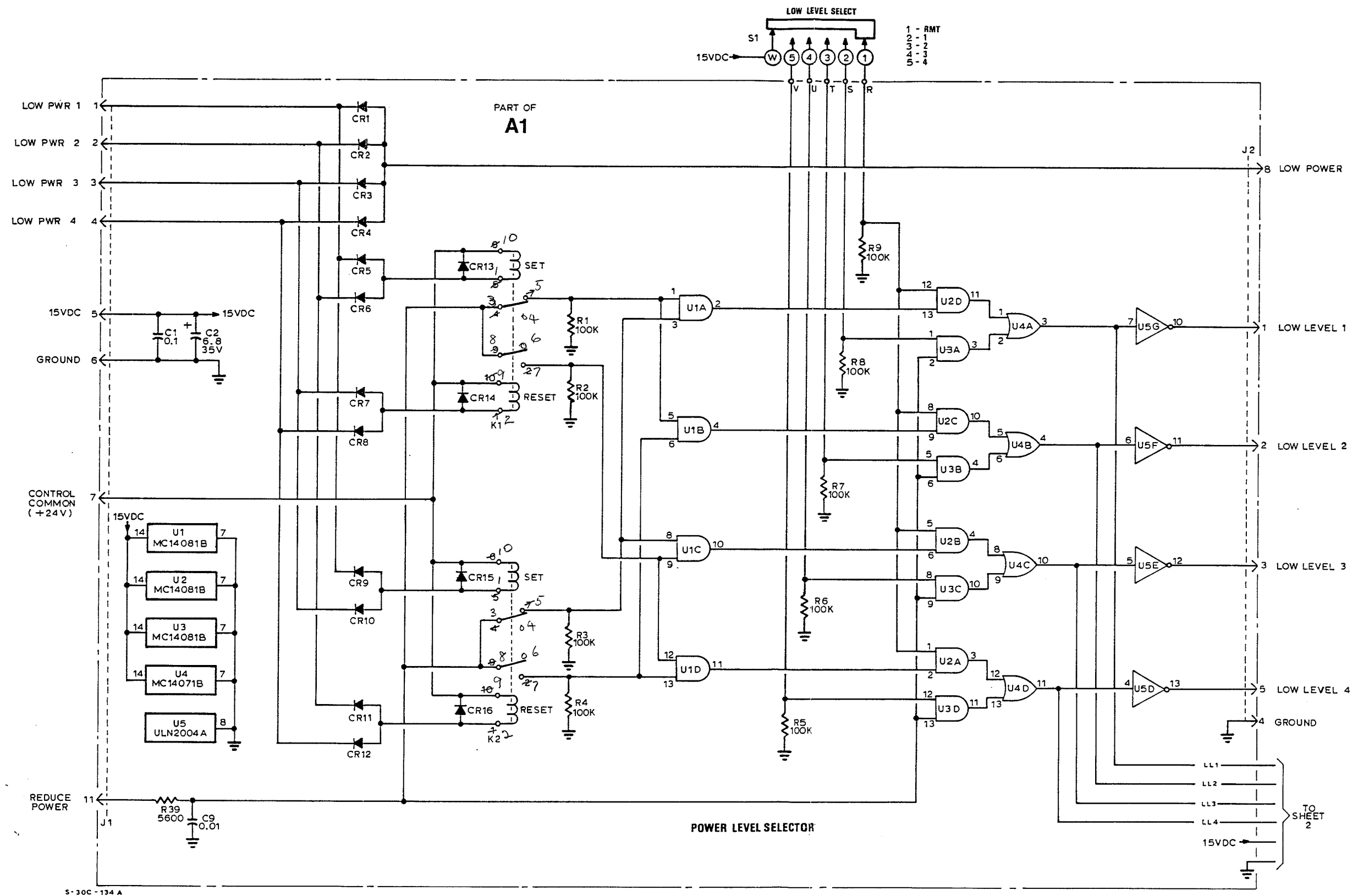


Figure 1 Test Setup





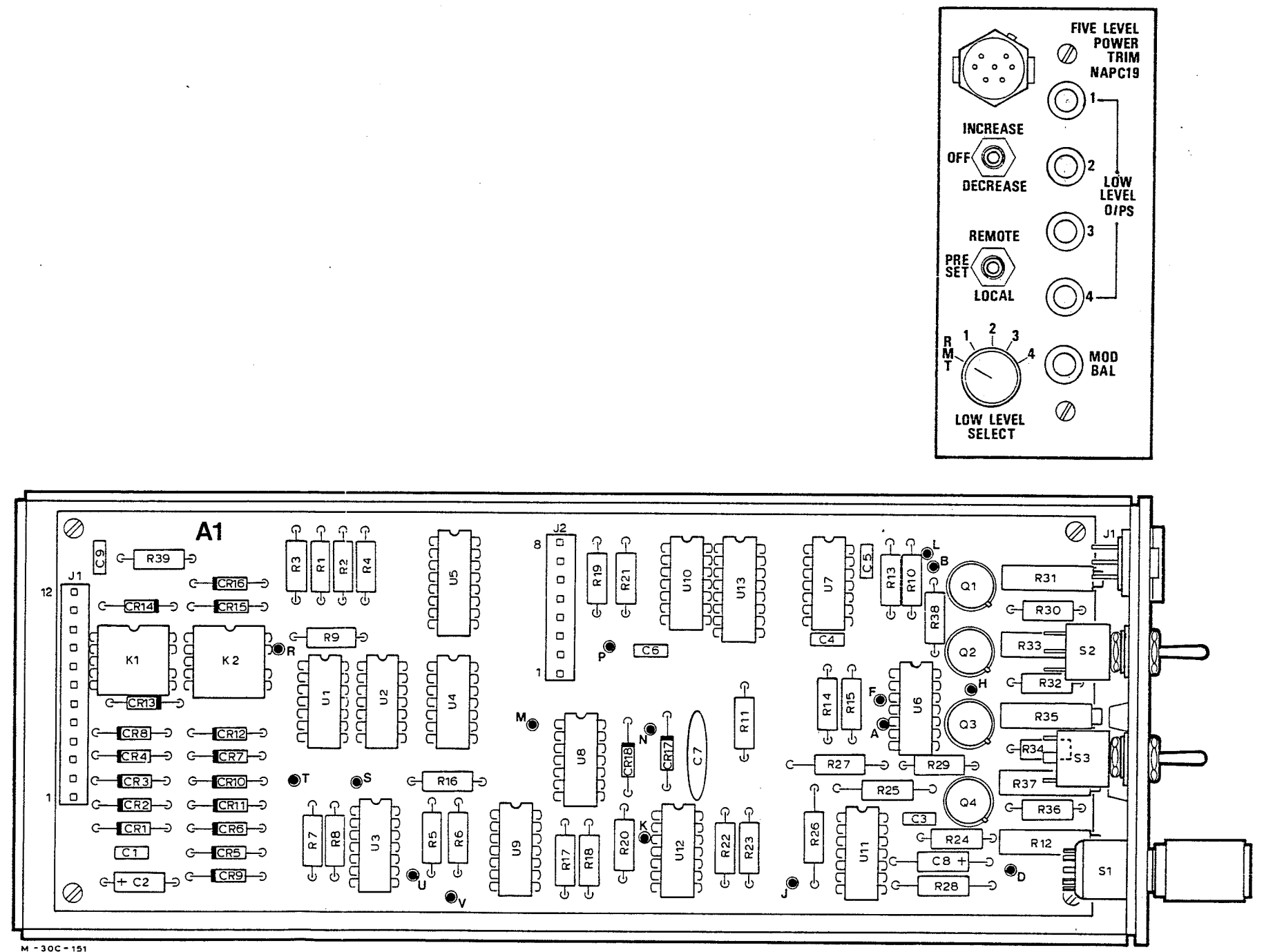


Figure FO-4 Assembly Detail - NAPC19 Five-Level Power Trim Assembly