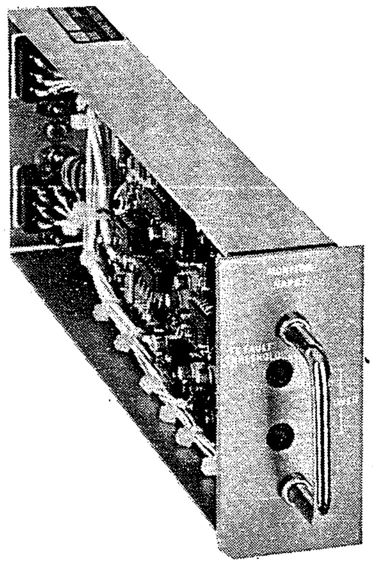
SERVICE INSTRUCTION

NAPC7

MONITOR MODULE



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LIST OF EFFECTIVE PAGES

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INTRODUCTION

1. The NAPC7 monitor module contains circuitry which monitors critical functions of Nautel's AMPFET series of transmitters and generates control signals to protect the transmitter when a fault condition exists. It also generates alarm signals for local and external monitoring, to alert users and maintainers a fault condition exists. Troubleshooting and repair of the module is performed on a work bench independent of its associated transmitter. This document provides the information required for a competent technician to understand the operation of the electrical circuits and the procedures to restore defective modules to a serviceable status; using tools and test equipment normally available at an AM radio station workshop. An alternative to procedures provided in this document is to utilize Nautel's module exchange/repair service facilities.

FACTORY EXCHANGE/REPAIR SERVICE

2. Nautel provides a factory, module exchange/repair service for users of Nautel's AMPFET series of transmitters. Users who do not have repair facilities or who are not able to repair a module may utilize this service for a nominal fee.

MECHANICAL CONFIGURATION

3. The NAPC7 monitor module utilizes a formed, metal box as the module chassis. Two electrical connectors and a guide pin are installed on the rear of the module; and a stamped panel containing a handle and two transmitter fault threshold adjustment access holes is installed on the front. All electrical components, except an inductor which is an integral part of the cable harness, are mounted on printed circuit board (A1). They are interconnected by the circuit board's printed pattern. Interconnecting wiring from the connectors is connected by soldering to standoff terminals on the circuit board. Refer to figure FO-4 for the assembly detail of the monitor module.

MONITOR MODULE OVERVIEW (figure FO-1)

4. Figure FO-1 depicts a block diagram of the NAPC7 monitor module. The following overview description is based on this illustration. Refer to paragraph 5 for a detailed description based on the electrical schematic shown in figures FO-2 and FO-3.

4.1 REFLECTED POWER MONITOR OVERVIEW: The reflected power monitor circuit monitors the 'reflected power' signal, from the associated transmitter's rf power probe. The 'reflected power' signal is a dc voltage that is proportional to the reflected power sensed at the transmitter's output. A 'high VSWR alarm' signal is produced when the reflected power exceeds four percent of the transmitter's rated power output. An analog dc voltage is also provided as the 'buffered reflected power' signal for remote monitoring purposes.

4.2 OUTPUT POWER MONITOR OVERVIEW: The output power monitor circuit monitors the 'forward power' signal, from the associated transmitter's rf power probe. The 'forward power' signal is a dc voltage that is proportional to the forward power output of the transmitter. A 'Tx fault alarm' signal is produced when the forward power falls below preset levels for high or low rf output power modes of operation. When a 'low power control' signal is applied, the high power reference level is inhibited and the low power reference level is selected. An analog dc voltage is also provided as the 'buffered forward power' signal for remote monitoring purposes.

4.3 PA FAILURE MONITOR OVERVIEW: The power amplifier failure monitor circuit monitors the current flow through the PA failure relays in the associated transmitter's modulator modules. It produces a 'PA failure alarm' signal when one or more of the relays energize and current flows in the 'PA fail sense' input. A 'PA fail pulse' is applied to the alarm cutback generator, during the initial surge of current when a relay is energized, to cutback the mod drive in the associated transmitter's mod driver module and to inhibit the rf drive during the relay contact make/break transition period.

4.4 24 VOLT DC MONITOR OVERVIEW: The 24 volt dc monitor circuit monitors the 24 volt dc power supply output and provides a 'mod drive enable' signal to the associated transmitter's modulator driver modules when the sensed voltage is greater than 19 volts dc. When the voltage falls below 19 volts dc, the 'mod drive enable' signal is removed and the transmitter's rf output will be inhibited.

4.5 HIGH TEMPERATURE MONITOR OVERVIEW: A thermistor, located in the airflow through the transmitter's power amplifier modules, provides a sensor for the high temperature monitor function. When the sensed temperature exceeds 75°C, the resistance of the thermistor will fall below the reference level and cause a 'high temp alarm' signal to be generated. This alarm signal will be maintained until the sensed temperature falls below 75°C and the transmitter is turned off and then on. A logic '1' 'high temp' signal is also produced and applied to the alarm cutback generator circuit when the sensed temperature is greater than 75°C. This signal will cause the mod drive, from the associated transmitter's mod driver module, to cutback until the sensed temperature falls below 75°C.

4.6 RF DRIVE MONITOR OVERVIEW: The rf drive monitor circuit monitors the 'rf drive sample' level. When this dc voltage falls below a fixed reference level, that represents the minimum acceptable rf drive, an 'rf drive standby alarm' and 'low rf drive' signals are generated. The 'rf drive standby alarm' signal initiates the changeover from main to standby rf drivers and also turns on an RF DRIVE alarm lamp in the associated transmitter. The 'low rf drive' signal, to the alarm cutback generator, inhibits the transmitter's rf output until the standby rf driver provides an rf drive that is greater than the fixed reference level. The 'rf drive standby alarm' and 'low rf drive' signals are inhibited by a control signal from the standby inhibit circuit when the transmitter is turned on, turned off or while resetting transmitter alarm circuits. This feature prevents changeover to standby or an inadvertent RF DRIVE alarm indication while the transmitters voltages are stabilizing.

4.7 MOD DRIVE MONITOR OVERVIEW: The mod drive monitor circuit monitors the 'mod drive alarm' signal from the transmitter's main modulator driver. When it is present, indicating a mod driver failure, a 'mod drive standby alarm' signal is generated. The 'mod drive standby alarm' signal initiates the changeover from main to standby modulator drivers and also turns on a MOD DRIVE alarm lamp in the associated transmitter. The 'mod drive standby alarm' signal is inhibited by a control signal from the standby inhibit function when the transmitter is turned on, turned off or while resetting transmitter alarm circuits. This feature prevents changeover to standby or an inadvertent MOD DRIVE alarm indication while the transmitters voltages are stabilizing.

4.8 ALARM CUTBACK GENERATOR OVERVIEW: The alarm cutback generator circuit is controlled by the status of the PA failure sensor, high temp monitor, rf drive monitor circuits and an external auxiliary alarm input. When a 'PA fail pulse' or an external 'aux alarm' input is applied, the alarm cutback generator produces a 50 millisecond 'alarm cutback' output. It also produces a continuous 'alarm inhibit' signal until the input signal is removed. When a 'high temp' or 'low rf drive' input is applied, the alarm cutback generator produces a continuous 'alarm cutback' output until the input signal is removed. When an 'alarm cutback' output is being produced, the mod drive from the associated transmitter's modulator driver is cut back and the rf output of the transmitter is reduced to a minimal level. When an 'alarm inhibit' signal is being produced, it will cause the rf drive inhibit circuit to inhibit the rf drive and the standby inhibit circuit to prevent changeover to mod/rf drive standby modules or the generation of a mod/rf drive alarm.

4.9 STANDBY INHIBIT OVERVIEW: The standby inhibit circuit monitors the '-72 vdc' input and produces a 'standby inhibit' command to the rf drive inhibit, rf drive monitor and mod drive monitor circuits when this voltage is less negative than -63 volts dc. It also generates a 'standby inhibit' command when an 'alarm inhibit' signal is being applied from the alarm cutback generator circuit. When a 'standby inhibit' command is being produced, it will cause the rf drive inhibit circuit to inhibit the rf drive and prevent changeover to the mod/rf drive standby modules or the generation of a mod/rf drive alarm.

4.10 RF INHIBIT GENERATOR OVERVIEW: The rf drive inhibit removes the 'rf drive enable' signal while a 'standby inhibit' or 'alarm inhibit' signal is being applied. When the 'rf drive enable' signal is removed, the rf carrier oscillator output of the associated transmitter's active rf driver is inhibited.

DETAILED THEORY OF OPERATION

5. The following description expands on the overview description presented in paragraph 4 and provides a detailed description of each function in the NAPC7 monitor module based on the electrical schematic depicted in figures FO-2 and FO-3.

5.1 REFLECTED POWER MONITOR DESCRIPTION: A 'reflected power' signal, which is a dc voltage that is proportional to the level of the reflected power sensed by the associated transmitter's rf power probe, is applied thru P2-7 to the inverting input of comparator U1B.

5.1.1 When the reflected power level is acceptable, the dc voltage applied to P2-7 will be less positive than the dc voltage on the non-inverting input of U1B, provided by voltage divider R5/R6/R7. U1B's output will be an open circuit to ground and 15 volts dc will be applied thru R9 to the inverting input of comparator U1D. The inverting input of U1-D will be more positive than the voltage on its non-inverting input, provided by voltage divider R10/R11. U1D's output will be a low resistance (forward diode resistance) to ground. The junction of R12/R13 will be clamped to ground, causing transistor Q1 to be reverse biased (turned off). The 'SWR alarm' output on P2-3 will be an open circuit.

5.1.2 When the reflected power level is not acceptable, the dc voltage applied to P2-7 will be more positive than the dc voltage on the non-inverting input of U1B. U1B's output will be a low impedance (forward diode resistance) to ground causing the inverting input of U1D to be clamped to ground. U1D's output will be an open circuit to ground and 15 volts dc will be applied to the base of transistor Q1. Q1 will be forward biased (turned on), and a ground will be applied to P2-3 as the 'SWR alarm' signal to the transmitters SWR ALARM lamp.

5.1.3 The dc voltage applied to P2-7 is also applied thru voltage divider R2/R3 to the non-inverting input of comparator U1A, which is connected as a follower amplifier. The resultant dc voltage is smoothed to the average value of the detected reflected power by capacitor C2 and resistor R4. The output of U1A will follow changes in the 'reflected power' signal and will be a dc voltage which is 0.924 of its level. U1A's output is applied to P1-9 as the 'buffered reflected power' output for application to a monitoring circuit which is remote from the associated transmitter.

5.2 OUTPUT POWER MONITOR DESCRIPTION: A 'forward power' signal, which is a dc voltage that is proportional to the level of the forward power sensed by the associated transmitter's rf power probe, is applied to P2-9. This dc voltage is filtered of any modulation component, smoothed to the average value of the forward power level by capacitor C5 and resistor R20 and applied to the non-inverting input of comparators U2B, U2C and U2D.

5.2.1 High Power Operation: When the transmitter is operating in its high power mode, the 'low power' input applied to P2-10 will be an open circuit (zero volts) and transistor Q2 will be reverse biased (turned off). 15 volts dc will be applied to voltage divider R14/R15/R16. The wiper of HIGH POWER potentiometer R15 is adjusted to apply a voltage that represents the fault threshold for the high, forward power output to the inverting input of U2C.

5.2.1.1 When the forward power is above the high power fault threshold level, the smoothed dc voltage applied to the non-inverting input of comparator U2C will be more positive than the threshold voltage on U2C's inverting input. U2C's output will be an open circuit to ground. 15 volts dc will be applied thru R23 to the base of transistor Q3 causing it to be forward biased (turned on). A ground will be applied to P1-5 as the 'tx fault alarm' signal. When a ground potential 'tx fault alarm' signal is applied to P1-5, it energizes the associated transmitter's tx fault relay, which inhibits the remote transmitter fault alarm indication.

NOTE

The transmitter's tx fault relay is connected as a fail safe relay. It is held energized when a fault does not exist and de-energizes when a fault occurs that affects the forward power level.

5.2.1.2 When the forward power falls below the high power fault threshold level, the smoothed dc voltage applied to the non-inverting input of comparator U2C will be less positive than the threshold voltage on U2C's inverting input. U2C's output will be a low impedance (forward diode resistance) to ground. The base of Q3 will be clamped to ground, causing it to be reverse biased (turned off). An open collector 'tx fault alarm' signal will be applied to P1-5. The associated transmitter's tx fault relay will de-energize and cause a remote transmitter fault alarm indication to be generated.

5.2.2 Low Power Operation: When the associated transmitter is operating in a low power mode, a 15 volt dc 'low power' signal will be applied to P2-10. Transistor Q2 will be forward biased (turned on). The junction of R14/R15 will be clamped to ground and effectively clamp the wiper of HIGH POWER potentiometer R15 and the inverting input of U2C to ground. U2C's output will be an open circuit to ground and it will have no influence on the status of transistor Q3. The wiper of LOW POWER potentiometer R22 is adjusted to apply a voltage that represents the fault threshold for the low, forward power output to the inverting input of U2B

5.2.2.1 When the forward power is above the low power fault threshold level, the smoothed dc voltage applied to the non-inverting input of comparator U2B will be more positive than the threshold voltage on U2B's inverting input. U2B's output will be an open circuit to ground. 15 volts dc will be applied thru R23 to the base of transistor Q3 causing it to be forward biased (turned on). A ground will be applied to P1-5 as the 'tx fault alarm' signal.

5.2.2.2 When the forward power falls below the low power fault threshold level, the smoothed dc voltage applied to the non-inverting input of comparator U2B will be less positive than the threshold voltage on U2B's inverting input. U2B's output will be a low impedance (forward diode resistance) to ground. The base of Q3 will be clamped to ground, causing it to be reverse biased (turned off). The 'tx fault alarm' signal to P1-5 will be an open collector. The associated transmitter's tx fault relay will de-energize and cause a remote transmitter fault alarm indication to be generated.

5.2.3 Buffered Forward Power: The filtered and smoothed dc voltage, from the junction of R20/C5 which represents the average forward power level, is also applied to the non-inverting input of comparator U2D. U2D is connected as a follower amplifier and provides a dc voltage output which is 0.924 (determined by voltage divider R19/R21) of the dc voltage applied to P2-9. U2D's output is applied to P1-11 as the 'buffered forward power' output for application to a monitoring circuit which is remote from the associated transmitter.

5.3 PA FAILURE SENSOR DESCRIPTION: The 'PA fail sense' input to P2-4 is actually the voltage source for power amplifier fault relays in the associated transmitter's modulator modules. Whenever a power amplifier fault occurs, a ground is applied to one of these relays and current will flow thru P2-4, R25, L2 and P2-11. During the initial current surge, a voltage pulse will be developed across L2. Transistor Q5 will be forward biased (turned on) for the duration of the voltage pulse and current will flow thru R26, R27 and Q5.

5.3.1 The resultant positive voltage pulse at the junction of Q5 collector/R26 will be applied to thyristor Q6 and cause Q6 to turn on and remain on. A ground will be applied thru Q6 to P2-5 as the 'PA fail alarm' signal and turn on the associated transmitter's PA FAIL alarm lamp. Thyristor Q6 will remain on until it is reset by turning the transmitter off, then on.

5.3.2 The positive voltage pulse at the junction of R26/R27 is applied to one input of OR gate U4B, of the alarm cutback generator circuit, as a logic '1' input. This logic '1' input will initiate an 'alarm cutback' output from the alarm cutback generator circuit and remove the rf drive enable output from the rf drive inhibit circuit during the modulator's relay contact make/break transition period.

5.4 24 VOLT DC MONITOR DESCRIPTION: The 24 volt dc monitor circuit inhibits the transmitter's mod driver modules whenever the unregulated 24 volt dc output of the low voltage power supply modules, which is applied to P2-11, is not acceptable.

5.4.1 When the voltage applied to P2-11 is more than 18 volts dc, CR3 will breakdown and current will flow thru R28/CR3. The junction of CR3/R28 will be a dc voltage that is sufficiently positive to forward bias (turn on) transistor Q4. A ground potential (logic '0') will be applied to the input gates of U3D thru Q4. U3D's output to P1-12 will be 15 volt dc ('logic 1') 'mod drive enable' signal. The output of the associated transmitter's modulator driver modules will be enabled.

5.4.2 When the voltage applied to P2-11 is less than 18 volts dc, CR3 will not breakdown and the junction of CR3/R28 will be at ground potential. Transistor Q4 will be reverse biased (turned off). 15 volts dc ('logic 1') will be applied to the input gates of U3D thru R53. U3D's output to P1-12 will be a ground potential ('logic 0') 'mod drive enable' signal. The output of the associated transmitter's modulator driver modules will be inhibited.

5.5 HIGH TEMPERATURE MONITOR DESCRIPTION: A thermistor, which has a negative temperature coefficient, is located in the airflow of the associated transmitter's power amplifier modules. The thermistor has a nominal resistance of 350 ohms when the sensed temperature is 75°C. It is connected between P1-2 and ground, as the 'high temp detect' input, and forms part of a voltage divider to 15 volts dc with resistor R45.

5.5.1 Temperature Less Than 75°C: When the sensed temperature is less than 75°C, the resistance of the thermistor will be more than 350 ohms. The dc voltage on the inverting input of comparator U2A; from the junction of R45/C15, will be 1.5 volts dc or greater. The voltage on the non-inverting input of U2A, from the junction of R46/R47, is dependent on the charging current thru C16 or the status of U2A. The initial charge current thru C16/R47/R46 will cause a nominal 1.5 volts dc to be applied to the non-inverting input of U2A, from the junction of R47/R46. Since this voltage is less positive than the dc voltage on U2A's inverting input, the output of U2A will be a low impedance (forward diode resistance) to ground. The junction of R47/C16 will be clamped to ground and maintain the junction of R46/47 at 1.5 volts dc. U2A's output will be maintained at ground potential (logic '0').

5.5.2 Temperature More Than 75°C: When the sensed temperature goes higher than 75°C, the resistance of the thermistor will decrease to a value of less than 350 ohms. The dc voltage applied to the inverting input of comparator U2A; from the junction of R45/C15, will be less than 1.5 volts dc. The voltage on the inverting input of U2A will be less positive than the 1.5 volts dc being maintained on U2A's non-inverting input, from the junction of R46/R47. U2A's output will switch to a high impedance (open circuit) and allow C16 to charge exponentially towards 15 volts dc. As C16 charges towards 15 volts dc, the voltage applied to U2A's non-inverting input, from the junction of R46/R47, will increase proportionally until it eventually stabilizes at 15 volts dc. When U2A's non-inverting input is being held at 15 volts dc, it is not possible for the voltage on its inverting input to go to a more positive voltage. U2A's output will be an open circuit status, regardless of the sensed temperature, until the temperature falls below 75°C and the circuit is reset by switching the transmitter off, then on. The voltage on C16 is applied to voltage divider R48/R49 and to U4A-3 in the alarm cutback generator circuit. When the voltage on C16 exceeds a nominal 10 volts dc, indicating an excessive temperature has been sensed, a logic '1' signal will be applied to U4A-3 and cause an 'alarm cutback' output to be produced. At the same time, the voltage at the junction of R48/R49 will be sufficiently positive to forward bias (turn on) thyristor Q10. Q10 will latch on and provide a ground potential 'high temp alarm' signal at P1-3 to turn on the transmitter's HIGH TEMP alarm lamp. Q10 will remain latched on until the circuit is reset by switching the transmitter off, then on.

5.6 RF DRIVE MONITOR DESCRIPTION: An 'rf drive sample' signal, which is a dc voltage that is proportional to the amplitude of the rf drive voltage being applied to the transmitter's power amplifiers, is applied to P2-6. A dc voltage, which represents the low rf drive reference threshold is applied to the non-inverting input of comparator U1C from voltage divider R33/R34.

5.6.1 When the rf drive amplitude is acceptable, the voltage applied to P2-6 will be greater than 35 volts dc. The resultant voltage at the junction of R31/R32, which is applied to the inverting input of comparator U1C, will be more positive than the voltage applied to U1C's non-inverting input, from the junction of R31/R32. U1C's output will be a low resistance (forward diode resistance) to ground. This ground potential is applied to U5D-13 and U4A-2, of the alarm cutback generator circuit, as a logic '0' input.

5.6.2 When the rf drive amplitude is not acceptable, the voltage applied to P2-6 will be less than 35 volts dc. The voltage applied to U1C's inverting input, from the junction of R31/R32, will be less positive than the voltage applied to its non-inverting input. U1C's output will switch to a high impedance (open circuit). 15 volts dc will be applied to U4A-2, of the alarm cutback generator circuit, and U5D-13 as a logic '1' input. U1C's output will be maintained as an open circuit until the rf drive is restored to an acceptable amplitude.

5.6.3 During the period of time a logic '1' is applied to U4A-2, an 'alarm cutback' output will be produced by the alarm cutback generator circuit.

5.6.4 The logic level on U5D-12 is dependent on the output status of the standby inhibit circuit. When the standby inhibit circuit's output is a logic '0' (ground potential), indicating the rf drive has been intentionally inhibited, U5D's output will be clamped to a logic '0' output and will not be influenced by logic level changes on U5D-13. When the standby inhibit circuit's output is a logic '1' (15 volts dc), indicating the rf drive is not being intentionally inhibited, U5D's output will follow logic level changes applied to U5D-13 from U1C.

5.6.4.1 When U5D's output is a logic '0', thyristor Q7 will be reverse biased (turned off) and apply an open circuit output to P1-6 as the 'rf drive alarm' output. The transmitter's RF DRIVE alarm lamp will not be turned on.

5.6.4.2 When U5D's output is a logic '1', thyristor Q7 will be forward biased (turned on) and apply a ground potential 'rf drive alarm' signal to P1-6. A ground potential 'rf drive standby alarm' signal will turn on the transmitter's RF DRIVE alarm lamp and will cause the main rf driver to be switched off the standby rf driver to be switched on. This condition will be maintained until the circuit is reset by switching the transmitter off, then on.

5.7 MOD DRIVE MONITOR DESCRIPTION: The 'mod drive alarm' input applied to P1-4 will be 15 volts dc (logic '1') when the pulse width modulated output (mod drive) of the active modulator driver is being applied to the transmitter's modulator modules or an open circuit (logic '0') when it is being inhibited.

5.7.1 When the 'mod drive alarm' input is a logic '1', transistor Q9 will be forward biased (turned on). A ground potential (logic '0') will be applied thru Q9 to U5A-1.

5.7.2 When the 'mod drive alarm' signal is a logic '0', transistor Q9 will be reverse biased (turned off). 15 volts dc (logic 1') will be applied thru R51 to U5A-1.

5.7.3 The logic level on U5A-2 is dependent on the output status of the standby inhibit circuit. When the standby inhibit circuit's output is a logic '0' (ground potential), indicating the rf drive has been intentionally inhibited, U5A's output will be clamped to a logic '0' output and will not be influenced by logic level changes on U5A-1. When the standby inhibit circuit's output is a logic '1' (15 volts dc), indicating the rf drive is not being intentionally inhibited, U5A's output will follow logic level changes on U5A-1.

5.7.3.1 When U5A's output is a logic '0', thyristor Q11 will be reverse biased (turned off) and apply an open circuit output to P2-2 as the 'mod driver alarm' output. The transmitter's MOD DRIVE alarm lamp will not be turned on.

5.7.3.2 When U5A's output is a logic '1', transistor Q11 will be forward biased (turned on) and apply a ground potential 'mod driver alarm' output to P2-2. A ground potential 'mod driver standby alarm' signal will turn on the transmitter's MOD DRIVE alarm lamp and will cause the main modulator driver to be switched off the standby modulator driver to be switched on. This condition will be maintained until the circuit is reset by switching the transmitter off, then on.

5.8 ALARM CUTBACK GENERATOR DESCRIPTION: The alarm cutback generator circuit applies a 15 volt dc (logic '1') 'alarm cutback' output to P1-8, for the required duration, whenever the monitoring circuits determine the transmitter's rf output must be cut back to a minimal level. It also produces a logic '0' output, which is applied to the standby inhibit and the rf inhibit circuits, when the rf drive is to be intentionally inhibited and to prevent the transfer from the main to the standby rf drive or mod drive modules.

5.8.1 Gates U4B and U3B, in conjunction with C9, CR4 and R37, form a one-shot multivibrator that produces a 50 millisecond logic '1' pulse at the output of U3B whenever a logic '1' input is applied to U4B-11 from the PA failure sensor circuit or to U4B-12 from P2-1 ('aux alarm' input). The output of U3B, which is applied to U4A-4/5, will be a logic '1' during this 50 millisecond period and will be a logic '0' for the remainder of the time.

5.8.2 Gates U4A and U3C form a buffered-output OR gate that applies a logic '1' 'alarm cutback' output to P1-8, from U3C-10 whenever a logic '1' input is being applied to U4A-2, from the rf drive monitor circuit, to U4A-3 from the high temp monitor circuit or to U4A-4/5 from U3B-4. The 'alarm cutback' output is applied to the transmitter's modulator driver modules and cuts back the pulse width modulation output (mod drive), and therefore the transmitter's rf output, to a minimal level when it is a logic '1'. When the 'alarm cutback' output is restored to a logic '0' level, the mod drive will return to its original level.

5.8.3 Gate U4B, in conjunction with U5B, forms a buffered-output NOR gate that produces a logic '0' output on U5B-4 whenever a logic '1' input is applied to U4B-11 or to U4B-12. This output logic level will be maintained for 50 milliseconds or the full period of time the logic '1' input is applied, whichever is longer. The output of U5B is applied to U3A-1, of the rf drive inhibit circuit, to inhibit, the transmitter's rf drive. It is also applied thru CR6/CR5 to U5C-8/9, of the standby inhibit circuit, to prevent the transfer from the main to standby rf drive/mod drive modules.

5.9 STANDBY INHIBIT DESCRIPTION: The standby inhibit circuit produces a logic '0' output at U5C-10, to inhibit the transfer-to-standby function of the rf drive monitor and mod drive monitor circuits, and a logic '0' output at the collector of Q8, to inhibit the transmitter's rf drive, when the negative voltage being applied to P1-1 is less than -63 volts dc. It also produces a logic '0' output at U5C-10, to inhibit the transfer-to-standby function of the rf drive monitor and mod drive monitor circuits, whenever a logic '0' input is being applied from the alarm cutback generator circuit.

5.9.1 Resistors R39/R40 form a voltage divider between +15 volts dc and the negative dc voltage applied to P1-1 from the transmitter's -72 volt dc power supply. At initial turn on, this negative voltage will increase exponentially towards -72 volts dc, as the storage capacitors in the transmitter's modulators are charged.

5.9.1.1 When the voltage applied to P1-1 is less negative than -63 volts dc, the junction of R39/R40 will be a positive voltage. Transistor Q8 will be forward biased (turned on) and its collector will be held at ground potential (logic '0'). This logic '0' will be applied to U3A-2 of the rf drive inhibit circuit to inhibit the rf drive it will also be applied to the integrator input of U5C.

5.9.1.1 When the voltage applied to P1-1 is more negative than -63 volts dc, the voltage at the junction of R39/R40 will reverse bias (turn off) transistor Q8. Q8's collector will go to 15 volts dc (logic '1'), provided a logic '0' is not being applied to Q8's collector thru CR6. This logic '1' will be applied to U3A-2 to enable the transmitter's rf drive and to the integrator input of U5C.

5.9.2 Resistors R5/R42 and capacitor C12 form an integrator circuit that has a fast attack/slow recovery time. When the integrator input is a logic '0', C12 will instantly discharge to ground (logic '0'). When the integrator input switches to a logic '1', C12 will charge exponentially towards a logic '1' level (nominally 10 volts dc) thru R41/R42. The output the integrator, which is the charge status of C12, is applied to the inputs of AND gate U5C. U5C's output, which is applied to U5A-2 of the mod drive monitor circuit and to U5D-12 of the rf drive monitor circuit, will follow logic level changes on its inputs.

5.9.2.1 When U5C's output is a logic '0', the transfer-to-standby function of the rf drive monitor and mod drive monitor circuits will be inhibited, regardless of the state of their respective monitoring circuits.

5.9.2.2 When U5C's output is a logic '1', the transfer-to-standby function of the rf drive monitor and mod drive monitor circuits will be enabled and they will respond to logic level changes in their respective monitoring circuits.

5.10 RF DRIVE INHIBIT DESCRIPTION: The rf drive inhibit circuit applies a ground potential ('logic 0') 'rf drive enable' output to P1-7, when it is safe for the transmitter's rf drive to be produced/applied to its power amplifier stages. When it is not safe to produce the rf drive, the rf drive inhibit circuit will apply a 15 volt dc (logic '1') 'rf drive enable' output to P1-7.

5.10.1 When the output of U5B and the collector of Q8 are both at a logic '1' level, the output of NAND gate U3A will be maintained at a logic '1' level and cause the transmitter's rf drive to be enabled.

5.10.1 When Q8's collector is a logic '0', indicating the negative voltage being applied to P1-1 is less than -63 volts dc, and/or the output of U5B is a logic '0', indicating a power amplifier failure has just been sensed or an external 'aux alarm' signal is being applied to P2-1, the output of NAND gate U3A will be a logic '0' level and cause the transmitter's rf drive to be inhibited.

TROUBLESHOOTING

6. Troubleshooting of monitor modules that are defective or are suspected of being defective consists of performing a visual inspection and then conducting a functional test to isolate the defective components.

6.1 TEST EQUIPMENT AND SPECIAL TOOLS: The test equipment required is listed in table 1. There are no special tools required.

6.2 VISUAL INSPECTION: It is recommended that a visual inspection be performed on the monitor module prior to applying power. Inspect the module for the following:

(a) Inspect all electrical components for evidence of overheating or physical damage.

(b) Inspect all solder connections for good mechanical bond and adequate solder.

(c) Verify connectors P1 and P2 do not contain damaged or loose pins and that they are securely fastened to the chassis.

(d) Verify the guide pin is present and that it is securely fastened.

(e) Verify all wiring insulation is not pinched, frayed, broken or otherwise damaged.

(f) Verify wire strands of wiring conductors are not broken or otherwise damaged.

(g) Verify the chassis and printed circuit board is free from solder slivers and other conductive foreign objects.

(h) Verify all integrated circuit devices are installed and firmly seated in their sockets.

(i) Verify all fastening hardware is securely tightened.

6.3 CALIBRATION/FUNCTIONAL TEST: Functional testing and calibration of the monitor module is the recommended first step in troubleshooting a defective module and also verifies the module is operating within design limits after corrective action has been taken. Modules that meet the requirements of the functional test may be considered to be operating satisfactorily and returned to service.

NOTE

Final testing and adjustment of the monitor module is performed with the module installed in the transmitter it will be used in. Instructions are provided in the associated transmitter's instruction manual.

The input or output of some steps specify logic levels. When a logic '0' level is specified, the voltage must be between zero volts and 5.0 volts dc. When a logic '1' level is specified, the voltage must be between 10.0 volts and 15.0 volts dc.

6.3.1 Preparation for Test/Calibration: Prepare the monitor module for test as follows:

(a) Verify the visual inspection has been completed.

(b) Connect the NAPC7 monitor module to the test setup depicted in figure 1.

(c) Set test setup's switches to positions shown in figure 1.

(d) Set test setup's REFL PWR potentiometer to its maximum counter clockwise position (minimum voltage to P2-7).

(e) Set test setup's FWD PWR potentiometer to its maximum clockwise position (15 volts dc to P2-9).

(f) Set test setup's HIGH TEMP potentiometer to its maximum clockwise position (maximum resistance).

(g) Switch on test setup's 15 volt dc power supply and verify its output is 14.3 volts dc.

(h) Set test setup's 15 VDC switch to its on position.

(i) All test setup alarm lamps shall be off.

6.3.2 Reflected Power Monitor Test: Check the operation of the reflected power monitor circuit as follows:

(a) Connect a digital voltmeter between the wiper (+) of test setup's REFL PWR potentiometer and chassis ground (-).

(b) Slowly adjust test setup's REFL PWR potentiometer clockwise (increasing voltage to P2-7), until test setup's SWR lamp just turns on.

(c) Indication on digital voltmeter shall be between 2.23 and 2.47 volts dc.

(d) Set test setup's REFL PWR potentiometer to its maximum counter clockwise position (minimum voltage to P2-7).

(e) Test setup's SWR alarm lamp shall turn off.

(f) Connect a second digital voltmeter between P1-9 (+), REFL PWR test point of test setup, and chassis ground (-).

(g) Simultaneously monitor both digital voltmeter indications while slowly adjusting test setup's REFL PWR potentiometer from its maximum counter clockwise position to its maximum clockwise position.

(h) Indication on voltmeter connected to REFL PWR test point shall follow changes but be nominally 10% less than indication on voltmeter connected to wiper of REFL PWR potentiometer.

(i) Set REFL PWR potentiometer of test setup to its maximum counter clockwise position (minimum voltage to P2-7).

(j) Disconnect digital voltmeters.

6.3.3 Output Power Monitor Test: Check the operation of the output power monitor circuit as follows:

(a) Set HIGH POWER - TX FAULT THRESHOLD potentiometer R15 fully clockwise.

(b) Set LOW POWER - TX FAULT THRESHOLD potentiometer R22 fully clockwise.

(c) Connect a digital voltmeter between the wiper (+) of test setup's FWD PWR potentiometer and chassis ground (-).

(d) Set test setup's FWD PWR potentiometer for a digital voltmeter indication of 9.5 volts dc.

(e) Slowly adjust HIGH POWER - TX FAULT THRESHOLD potentiometer R15 counter clockwise until test setup's TX FAULT lamp just turns ~~on.~~ off

(f) HIGH POWER - TX FAULT THRESHOLD potentiometer R15 should be in the approximate centre of its adjustment range (one half turn).

(g) Set HIGH POWER - TX FAULT THRESHOLD potentiometer R15 to its fully clockwise position.

(h) Test setup's TX FAULT lamp shall turn ~~off.~~ on

(i) Set test setup's FWD PWR potentiometer to its maximum clockwise position (15 volts dc to P2-9).

(j) Set test setup's LOW PWR switch to its closed position.

(k) Test setup's TX FAULT lamp shall remain ~~off.~~ on

(l) Set test setup's FWD PWR potentiometer for a digital voltmeter indication of 8.0 volts dc.

(m) Slowly adjust LOW POWER - TX FAULT THRESHOLD potentiometer R22 counter clockwise until test setup's TX FAULT lamp just turns ~~on.~~ off

(n) LOW POWER - TX FAULT THRESHOLD potentiometer R22 should be in the approximate centre of its adjustment range (one half turn).

(o) Set LOW POWER - TX FAULT THRESHOLD potentiometer R15 to its fully clockwise position.

(p) Test setup's TX FAULT lamp shall turn ~~off.~~ on

(q) Connect a second digital voltmeter between P1-11 (+), FWD PWR test point of test setup, and chassis ground (-).

(r) Simultaneously monitor both digital voltmeter indications while slowly adjusting test setup's FWD PWR potentiometer from its maximum clockwise position to its maximum counter clockwise position.

(s) FWD PWR test point voltmeter indication shall follow changes but be nominally 10% less than indication of voltmeter on wiper of FWD PWR potentiometer.

(t) Set test setup's LOW PWR switch to its open position and repeat steps (r) and (s).

(u) Set FWD PWR potentiometer of test setup to its maximum clockwise position (15 volts dc to P2-9).

(v) Disconnect digital voltmeters.

6.3.4 <u>24 Volt dc Monitor Test</u>: Check the operation of the 24 volt dc monitor circuit as follows:

(a) Connect a variable dc power supply that has been preset to 0.0 volts dc between P2-11 (+), 24 VDC test point of test setup, and chassis ground (-).

(b) Connect a digital voltmeter between P1-12 (+), MOD DRIVE ENABLE test point of test setup, and chassis ground (-).

(c) Digital voltmeter indication shall be a logic '0' level.

(d) Slowly increase output of variable dc power supply until voltmeter indication switches to a logic '1' level.

(e) Variable dc power supply output voltage shall be between 18.0 and 20.0 volts dc.

(f) Set output of variable dc power supply to 24.0 volts dc.

(g) Disconnect digital voltmeter.

6.3.5 <u>PA Failure Monitor Test</u>: Check the operation of the PA failure monitor circuit as follows:

(a) Verify a dc power supply has been connected between P2-11 (+), 24 VDC test point of test setup, and chassis ground (-); and that it has been preset to 24.0 volts dc.

(b) Set test setup's PA FAIL switch to its 24 VDC position.

(c) Connect an oscilloscope between P1-8 (+), ALARM CUTBACK test point of test setup, chassis ground (-).

(d) Simultaneously observe oscilloscope indication and set test setup's PA FAIL switch to its GND position.

(e) A single logic '1' level pulse, with a duration of 50 milliseconds, shall be observed on oscilloscope.

(f) Test setup's PA FAIL alarm lamp shall turn on and remain on.

(g) Set test setup's PA FAIL switch to its 24 volt dc position.

(h) Momentarily switch off test setup's 15 volt dc power supply and then switch it on.

(i) Test setup's PA FAIL alarm lamp shall turn off.

(j) Switch off and disconnect 24 volt dc power supply.

6.3.6 High Temperature Monitor Test: Check the temperature monitor circuit as follows:

(a) Verify test setup's HIGH TEMP potentiometer is set to its maximum clockwise position (maximum resistance).

(b) Verify an oscilloscope is connected between P1-8 (+), ALARM CUTBACK test point of test setup, chassis ground (-).

(c) Oscilloscope trace shall be at the logic '0' level.

(d) Slowly adjust test setup's HIGH TEMP potentiometer counter clockwise (decrease resistance) until test setup's HIGH TEMP alarm lamp just turns on.

(e) Oscilloscope trace shall switch to logic '1' level.

(f) Test setup's HIGH TEMP potentiometer's resistance shall be 350 ± 20 ohms.

(g) Set HIGH TEMP potentiometer to its maximum resistance (clockwise) position.

(h) Test setup's HIGH TEMP alarm lamp shall remain on and oscilloscope trace shall remain at a logic '1' level.

(i) Momentarily switch off test setup's 15 volt dc power supply and then switch it on.

(j) Test setup's HIGH TEMP alarm lamp shall turn off and oscilloscope trace shall return to a logic '0' level.

6.3.7 Standby Inhibit Test: Check the operation of the standby inhibit circuit as follows:

(a) Connect a variable dc power supply, that has been preset to 0.0 volts dc, between P1-1 (-), -72 VDC test point of test setup, and chassis ground (+).

(b) Connect a digital voltmeter between P1-7 (+), RF DRIVE ENABLE test point of test setup, and chassis ground (-).

(c) Connect an oscilloscope between A1U5-10 and chassis ground.

(d) Digital voltmeter indication shall be a logic '1' level and oscilloscope trace shall be at a logic '0' level.

(e) Simultaneously monitor voltmeter indication and oscilloscope trace and then slowly increase output of variable dc power supply until voltmeter indication switches to a logic '0' level.

(f) Oscilloscope trace shall switch to a logic '1' level approximately 500 milliseconds after voltmeter indication switches to a logic '0'.

(g) Test setup's RF DRIVE alarm lamp shall turn on and remain on.

(h) Variable dc power supply output voltage shall be between -60.0 and -66.0 volts dc.

(i) Switch off 15 volt dc power supply and variable dc power supply.

(j) Disconnect variable dc power supply, oscilloscope and digital voltmeter.

(k) Switch on 15 volt dc power supply. Test setup's RF DRIVE alarm lamp shall be off.

6.3.8 RF Drive Monitor Test: Check the rf drive monitor circuit as follows:

(a) Connect a variable dc power supply that has been preset to 40.0 volts dc between P2-6 (+), RF DRIVE test point of test setup, and chassis ground (-).

(b) Connect a shorting jumper wire across capacitor A1C11.

(c) Connect an oscilloscope between P1-8 (+), ALARM CUTBACK test point of test setup, and chassis ground (-).

(d) All alarm lamps of test setup shall be off and oscilloscope trace shall be a logic '0' level.

(e) Slowly decrease output of variable dc power supply connected to P2-6 until test setup's RF DRIVE alarm lamp just turns on.

(f) Oscilloscope trace shall switch to a logic '1' level.

(g) Variable dc power supply output voltage shall be between 34.0 and 36.0 volts dc.

(h) Set output of variable dc power supply connected to P2-6 to 40 volts dc.

(i) Oscilloscope trace shall switch to a logic '0' level and test setup's RF DRIVE alarm lamp shall remain on.

(j) Momentarily switch off test setup's 15 volt dc power supply and then switch it on.

(k) Test setup's RF DRIVE alarm lamp shall turn off and remain off.

6.3.9 Mod Drive Monitor Test: Check the modulator drive monitor circuit as follows:

(a) Verify a variable dc power supply that has been preset to 40.0 volts dc is connected between P2-6 (+), RF DRIVE test point of test setup, and chassis ground (-).

(b) Verify a shorting jumper wire is connected across capacitor C11.

(c) Verify an oscilloscope is connected between P1-8 (+), ALARM CUTBACK test point of test setup, and chassis ground (-).

(d) All test setup alarm lamps shall be off and oscilloscope trace shall be a logic '0' level.

(e) Set test setup's MOD DRIVE ALARM switch to its closed position.

(f) Test setup's MOD DRIVE alarm lamp shall turn on.

(g) Oscilloscope trace shall switch to a logic '1' level

(h) Set test setup's MOD DRIVE ALARM switch to its open position.

(i) Oscilloscope trace shall switch to a logic '0' level and test setup's MOD DRIVE alarm lamp shall remain on.

(j) Momentarily switch off test setup's 15 volt dc power supply and then switch it on.

(k) Test setup's MOD DRIVE alarm lamp shall turn off and remain off.

6.3.10 Alarm Cutback Generator Test: Check the the alarm cutback generator circuit as follows:

NOTE

The only function of the alarm cutback circuit that has not been tested by a previous test is the 'aux alarm' test. If they have not been previously completed, complete paragraphs 6.3.5, 6.3.6, 6.3.7 and 6.3.8.

(a) Verify a variable dc power supply that has been preset to 40.0 volts dc is connected between P2-6 (+), RF DRIVE test point of test setup, and chassis ground (-).

(b) Verify a shorting jumper wire is connected across capacitor C11.

(c) Verify an oscilloscope is connected between P1-8 (+), ALARM CUTBACK test point of test setup, and chassis ground (-).

(d) All alarm lamps of test setup shall be off and oscilloscope trace shall be a logic '0' level.

(e) Simultaneously monitor oscilloscope trace and set test setup's AUX ALARM switch to its closed position.

(f) A single logic '1' level pulse, with a duration of 50 milliseconds, shall be observed on oscilloscope.

(g) Switch off variable dc power supply connected between P2-6 and chassis ground (-). Disconnect variable dc power supply and oscilloscope.

6.3.11 RF Inhibit Generator Test: Check the rf inhibit generator circuit as follows:

(a) Connect or verify a shorting jumper wire is connected across capacitor C11.

(b) Connect an oscilloscope between P1-7 (+), RF DRIVE ENABLE test point of test setup, and chassis ground (-).

(c) Oscilloscope trace shall be at a logic '0' level.

(d) Simultaneously monitor oscilloscope trace and set test setup's AUX ALARM switch to its closed position.

(e) A single logic '1' level pulse, with a duration of 50 milliseconds, shall be observed on oscilloscope.

(f) Set test setup's AUX ALARM switch to its open position.

(g) Remove shorting jumper wire previously installed across capacitor C11.

(h) Oscilloscope trace shall switch to a logic '1' level.

(i) Disconnect oscilloscope.

6.4 COMPLETION OF TESTS: On the completion of the functional tests, switch off the 15 volt dc power supply and disconnect the monitor module from the test setup.

REPAIR

7. There are no special repair instructions. Observe normal care and precautions when handling CMOS solid state devices and removing and replacing components soldered to the printed pattern of printed circuit board A1.

NOTE

Refer to table 2 for interconnecting wiring information and to figure FO-4 for assembly detail of the monitor module.

Table 1 - Test Equipment

NOMENCLATURE	PART, MODEL, OR TYPE NUMBER (EQUIVALENTS MAY BE USED)
Digital Multimeter (2)	3 1/2 digit, ac and dc volts, ohms and amps, ±0.5% accuracy. Beckman 3010
Oscilloscope	15 MHz, Tektronics. Model T922
15 Vdc Power Supply	15 Volts 1 Amp
0-100 Vdc Power Supply	Continuously Variable
Test Setup	As depicted in figure 1.

Table 3 NAPC7 Reference Designation Index

REF DES	NAME OF PART AND DESCRIPTION	NAUTEL'S PART NO.	JAN, MIL OR MFR PART NO.
-	Monitor Module	NAPC7	139-3026-1
A1	Monitor Printed Circuit Board Assembly	139-3073	139-3073
A1C1	Capacitor, Tantalum, 6.8uF 10%, 35V	CCP19	CSR13F685KM
A1C2	Capacitor, Tantalum, 6.8uF 10%, 35V	CCP19	CSR13F685KM
A1C3	Capacitor, Tantalum, 1.0uF 10%, 50V	CCP24	CSR13G105KM
A1C4	Capacitor, Tantalum, 1.0uF 10%, 50V	CCP24	CSR13F105KM
A1C5	Capacitor, Tantalum, 6.8uF 10%, 35V	CCP19	CSR13F685KM
A1C6	Capacitor, Tantalum, 1.0uF 10%, 50V	CCP24	CSR13G105KM
A1C7	Capacitor, Ceramic, 0.01uF 10%, 100V	CCG04	CKR05BX103KL
A1C8	Capacitor, Ceramic, 0.22uF 10%, 50V	CCG08	CKR06BX224KL
A1C9	Capacitor, Ceramic, 0.1uF 10%, 100V	CCG07	CKR06BX104KL
A1C10	Capacitor, Tantalum, 6.8uF 10%, 6V	CCP01	CSR13B685KM
A1C11	Capacitor, Ceramic, 0.01uF 10%, 100V	CCG04	CKR05BX103KL
A1C12	Capacitor, Tantalum, 1.0uF 10%, 50V	CCP24	CSR13F105KM
A1C13	Capacitor, Tantalum, 1.0uF 10%, 50V	CCP24	CSR13G105KM
A1C14	Capacitor, Ceramic, 0.01uF 10%, 100V	CCG04	CKR05BX103KL
A1C15	Capacitor, Tantalum, 6.8uF 10%, 6V	CCP01	CSR13B685KM
A1C16	Capacitor, Tantalum, 1.0uF 10%, 50V	CCP24	CSR13G105KM
A1C17	Capacitor, Ceramic, 0.01uF 10%, 100V	CCG04	CKR05BX103KL
A1C18	Capacitor, Ceramic, 0.01uF 10%, 100V	CCG04	CKR05BX103KL
A1CR1	Diode	QAP29	1N4938
A1CR2	Diode	QAP29	1N4938
A1CR3	Diode, Zener, 18V, 1.5W, 10%	QK37	1N5931A
A1CR4	Diode	QAP29	1N4938
A1CR5	Diode	QAP29	1N4938
A1CR6	Diode	QAP29	1N4938
A1L1	Toroid	LY09	11-122-B
A1L2	Inductor	139-3036	139-3036
A1Q1	Transistor, NPN	QAP06	2N2222
A1Q2	Transistor, NPN	QAP06	2N2222
A1Q3	Transistor, NPN	QAP06	2N2222
A1Q4	Transistor, NPN	QAP06	2N2222
A1Q5	Transistor, PNP	QAP09	2N2907
A1Q6	Thyristor	QB16	MCR203
A1Q7	Thyristor	QB16	MCR203
A1Q8	Transistor, NPN	QAP06	2N2222
A1Q9	Transistor, NPN	QAP06	2N2222
A1Q10	Thyristor	QB16	MCR203
A1Q11	Thyristor	QB16	MCR203
A1R1	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R2	Resistor, Film, 8200 ohms, 2% 1/2W	RD06	RL20S822G
A1R3	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R4	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R5	Resistor, Film, 47K ohms, 2% 1/2W	RD15	RL20S473G
A1R6	Resistor, Film, 56K ohms, 2% 1/2W	RAP16	RL20S563G
A1R7	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G

Table 3 NAPC7 Reference Designation Index Module (Continued)

REF DES	NAME OF PART AND DESCRIPTION	NAUTEL'S PART NO.	JAN, MIL OR MFR PART NO.
A1R8	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R9	Resistor, Comp, 1.0M ohms, 5% 1/2W	RF31	RC20GF105J
A1R10	Resistor, Film, 56K ohms, 2% 1/2W	RAP16	RL20S563G
A1R11	Resistor, Film, 56K ohms, 2% 1/2W	RAP16	RL20S563G
A1R12	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R13	Resistor, Film, 5600 ohms, 2% 1/2W	RAP12	RL20S562G
A1R14	Resistor, Film, 2700 ohms, 2% 1/2W	RC42	RL20S272G
A1R15	Resistor, Variable, 10K ohms, 1/2W	RW27	63X103T000
A1R16	Resistor, Film, 5600 ohms, 2% 1/2W	RAP12	RL20S562G
A1R17	Resistor, Film, 56K ohms, 2% 1/2W	RAP16	RL20S563G
A1R18	Resistor, Film, 5600 ohms, 2% 1/2W	RAP12	RL20S562G
A1R19	Resistor, Film, 8200 ohms, 2% 1/2W	RD06	RL20S822G
A1R20	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R21	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R22	Resistor, Variable, 10K ohms, 1/2W	RW27	63X103T000
A1R23	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R24	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R25	Resistor, Film, 3.3 ohms, 2% 1/2W	RC07	A20-3.3 Ohms-2%
A1R26	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R27	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R28	Resistor, Film, 5600 ohms, 2% 1/2W	RAP12	RL20S562G
A1R29	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R30	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R31	Resistor, Film, 56K ohms, 2% 1/2W	RAP16	RL20S563G
A1R32	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R33	Resistor, Film, 33K ohms, 2% 1/2W	RAP15	RL20S333G
A1R34	Resistor, Film, 18K ohms, 2% 1/2W	RAP14	RL20S183G
A1R35	Resistor, Film, 33K ohms, 2% 1/2W	RAP15	RL20S333G
A1R36	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G
A1R37	Resistor, Comp, 1.0M ohms, 5% 1/2W	RF31	RC20GF105J
A1R38	Resistor, Film, 56K ohms, 2% 1/2W	RAP16	RL20S563G
A1R39	Resistor, Film, 10K ohms, 1% 1/2W	RZ10	RN60D1002F
A1R40	Resistor, Film, 45.3K ohms, 1% 1/2W	RY22	RN60D4532F
A1R41	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R42	Resistor, Comp, 1.0M ohms, 5% 1/2W	RF31	RC20GF105J
A1R43	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R44	Resistor, Film, 56K ohms, 2% 1/2W	RAP16	RL20S563G
A1R45	Resistor, Film, 3300 ohms, 2% 1/2W	RAP11	RL20S332G
A1R46	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R47	Resistor, Film, 1000 ohms, 2% 1/2W	RAP09	RL20S102G
A1R48	Resistor, Film, 33K ohms, 2% 1/2W	RAP15	RL20S333G
A1R49	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R50	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R51	Resistor, Film, 10K ohms, 2% 1/2W	RAP13	RL20S103G
A1R52	Resistor, Film, 5600 ohms, 2% 1/2W	RAP12	RL20S562G
A1R53	Resistor, Film, 100K ohms, 2% 1/2W	RAP17	RL20S104G

Table 3 NAPC7 Reference Designation Index Module (Continued)

REF DES	NAME OF PART AND DESCRIPTION	NAUTEL'S PART NO.	JAN, MIL OR MFR PART NO.
A1U1	IC, Comparator, Quad	UL02	MC3302
A1U2	IC, Comparator, Quad	UL02	MC3302
A1U3	IC, CMOS, Quad 2-input NAND Gates	UB03	MC14011BAL
A1U4	IC, CMOS, Dual, 4-input NOR Gates	UB02	MC14002BAL
A1U5	IC, CMOS, Quad, 2-input AND Gates	UB20	MC14081BAL
A1XU1	Socket, Integrated Circuit, 14-pin	UC02	640-357-1
A1XU2	Socket, Integrated Circuit, 14-pin	UC02	640-357-1
A1XU3	Socket, Integrated Circuit, 14-pin	UC02	640-357-1
A1XU4	Socket, Integrated Circuit, 14-pin	UC02	640-357-1
A1XU5	Socket, Integrated Circuit, 14-pin	UC02	640-357-1
L1	Toroid, Coated	LX13	11-762-B
P1	Connector, Plug, 12-pin	JD11	P-3312-AB
P2	Connector, Plug, 12-pin	JD11	P-3312-AB

Table 4 NAPC7 Parts Per Unit Index

NAUTEL'S PART NO.	NAME OF PART AND DESCRIPTION	JAN, MIL OR MFR PART NO.	(OEM) MFR CODE	TOTAL IDENT PARTS
NAPC7	Monitor Module	139-3026-1	37338	REF
139-3036	Inductor	139-3036	37338	1
139-3073	Monitor Printed Circuit Board Assembly	139-3073	37338	1
CCG04	Capacitor, Ceramic, 0.01uF 10%, 100V	CKR05BX103KL	56289	5
CCG07	Capacitor, Ceramic, 0.1uF 10%, 100V	CKR06BX104KL	56289	1
CCG08	Capacitor, Ceramic, 0.22uF 10%, 50V	CKR06BX224KL	56289	1
CCG09	Capacitor, Ceramic, 0.47uF 10%, 50V	CKR06BX474KL	56289	1
CCP01	Capacitor, Tantalum, 6.8uF 10%, 6V	CSR13B685KM	56289	2
CCP19	Capacitor, Tantalum, 6.8uF 10%, 35V	CSR13F685KM	56289	3
CCP24	Capacitor, Tantalum, 1.0uF 10%, 50V	CSR13G105KM	56289	6
JD11	Connector, Plug, 12-pin	P-3312-AB	13150	2
LX13	Toroid, Coated	11-762-B	33062	1
LY09	Toroid	11-122-B	33062	1
QAP06	Transistor, NPN	2N2222	04713	6
QAP09	Transistor, PNP	2N2907	04713	1
QAP29	Diode	1N4938	01295	5
QB16	Thyristor	MCR203	04713	4
QK37	Diode, Zener, 18V, 1.5W, 10%	1N5931A	04713	1
RAP09	Resistor, Film, 1000 ohms, 2% 1/2W	RL20S102G	36002	1
RAP11	Resistor, Film, 3300 ohms, 2% 1/2W	RL20S332G	36002	1
RAP12	Resistor, Film, 5600 ohms, 2% 1/2W	RL20S562G	36002	5
RAP13	Resistor, Film, 10K ohms, 2% 1/2W	RL20S103G	36002	16
RAP14	Resistor, Film, 18K ohms, 2% 1/2W	RL20S183G	36002	1
RAP15	Resistor, Film, 33K ohms, 2% 1/2W	RL20S333G	36002	3
RAP16	Resistor, Film, 56K ohms, 2% 1/2W	RL20S563G	36002	7
RAP17	Resistor, Film, 100K ohms, 2% 1/2W	RL20S104G	36002	7
RAP19	Resistor, Film, 330K ohms, 2% 1/2W	RL20S334G	36002	2
RC07	Resistor, Film, 3.3 ohms, 2% 1/2W	A20-3.3 Ohms-2%	36002	1
RC10	Resistor, Film, 5.6 ohms, 2% 1/2W	A20-5.6 Ohms-2%	36002	1
RC42	Resistor, Film, 2700 ohms, 2% 1/2W	RL20S272G	36002	1
RD06	Resistor, Film, 8200 ohms, 2% 1/2W	RL20S822G	36002	2
RD15	Resistor, Film, 47K ohms, 2% 1/2W	RL20S473G	36002	1
RF31	Resistor, Comp, 1.0M ohms, 5% 1/2W	RC20GF105J	36002	3
RW27	Resistor, Variable, 10K ohms, 1/2W	63X103T000	02111	2
RY22	Resistor, Film, 45.3K ohms, 1% 1/2W	RN60D4532F	36002	1
RZ10	Resistor, Film, 10K ohms, 1% 1/2W	RN60D1002F	36002	1
UB02	IC, CMOS, Dual, 4-input NOR Gates	MC14002BAL	04713	1
UB03	IC, CMOS, Quad 2-input NAND Gates	MC14011BAL	04713	1
UB20	IC, CMOS, Quad, 2-input AND Gates	MC14081BAL	04713	1
UC02	Socket, Integrated Circuit, 14-pin	640-357-1	00779	5
UL02	IC, Comparator, Quad	MC3302	04713	2

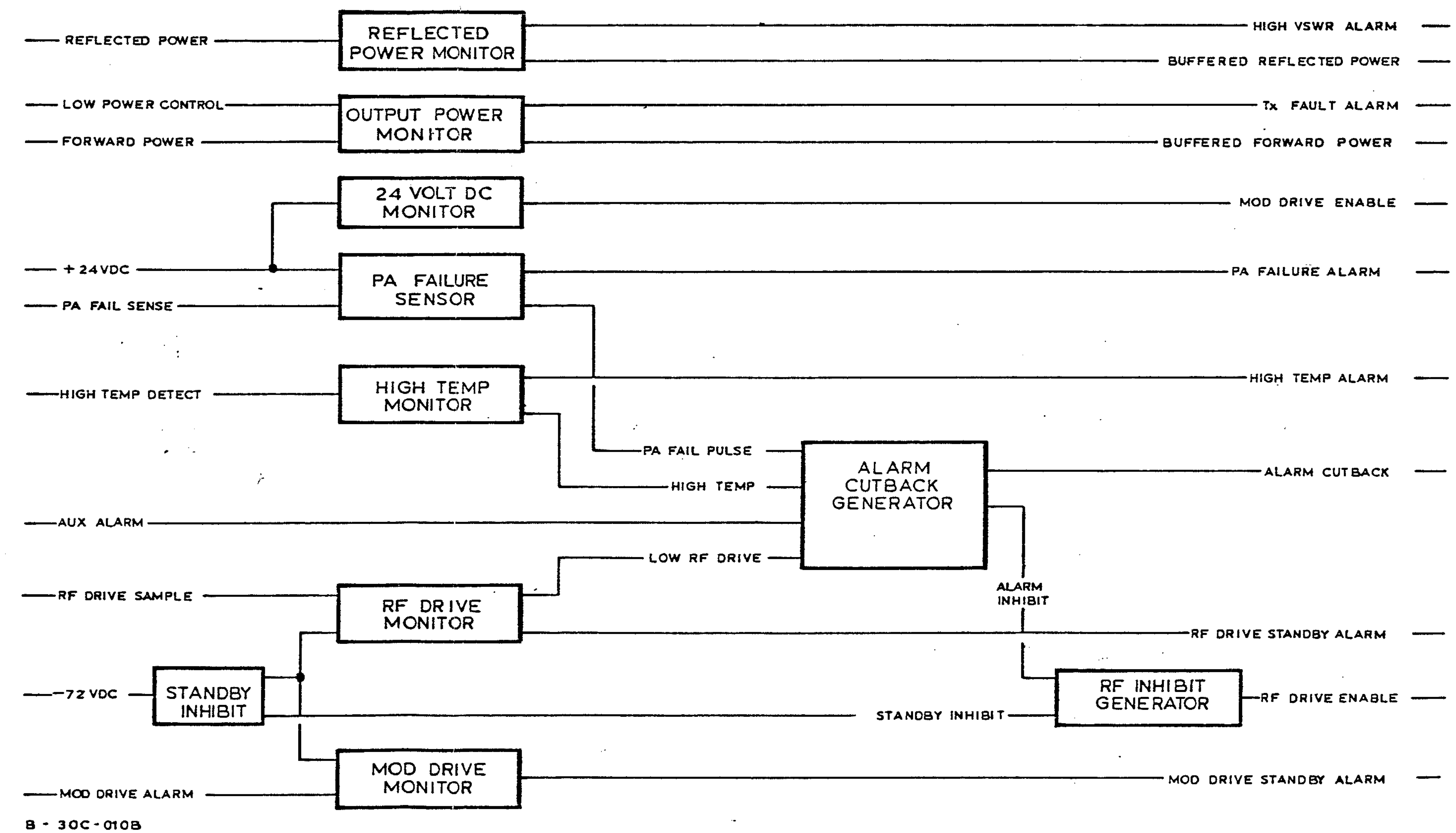

Figure FO-1 Block Diagram - NAPC7 Monitor Module

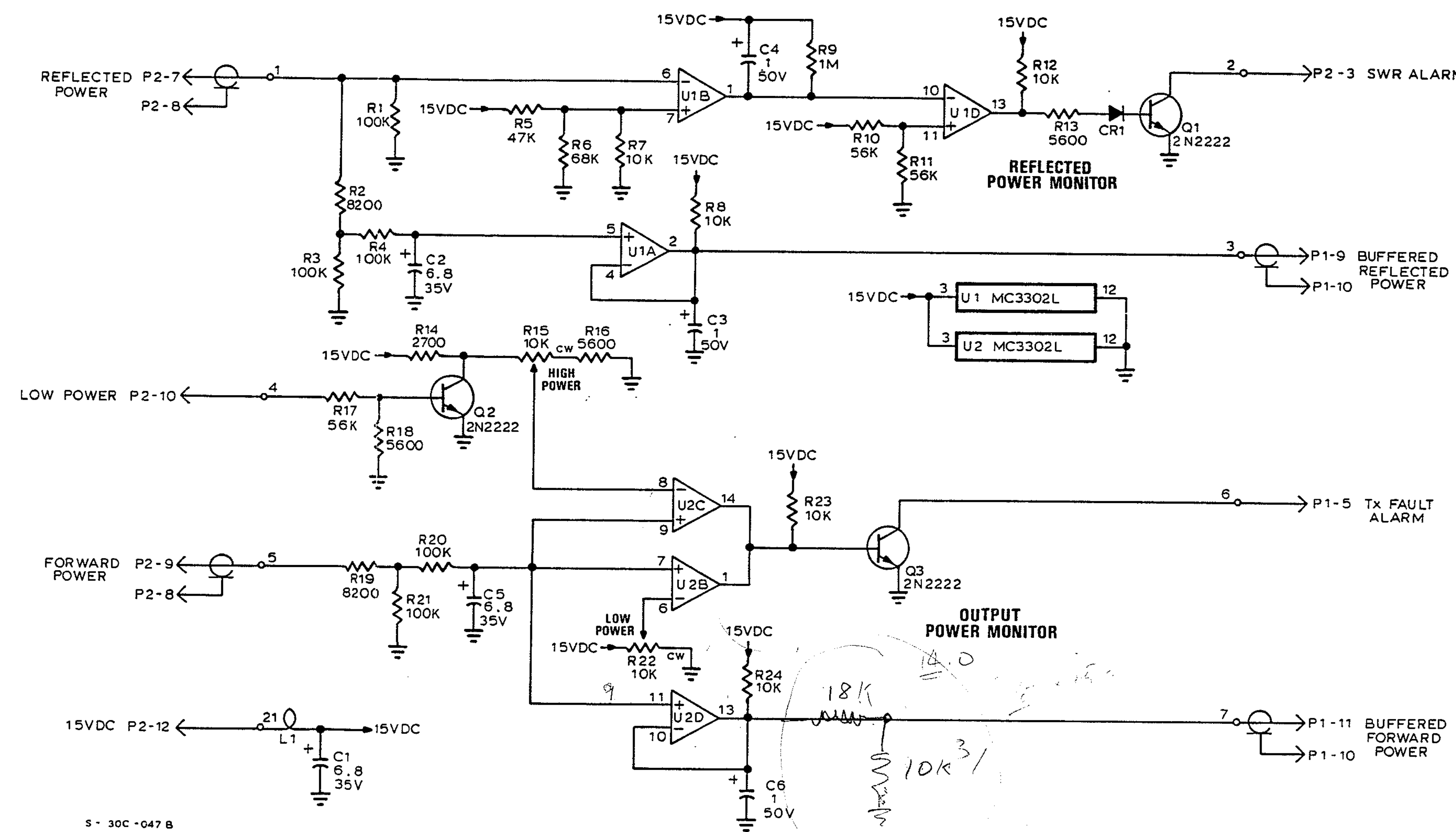

Figure FO-2 Electrical Schematic - NAPC7 Monitor Module (Sheet 1 of 2)

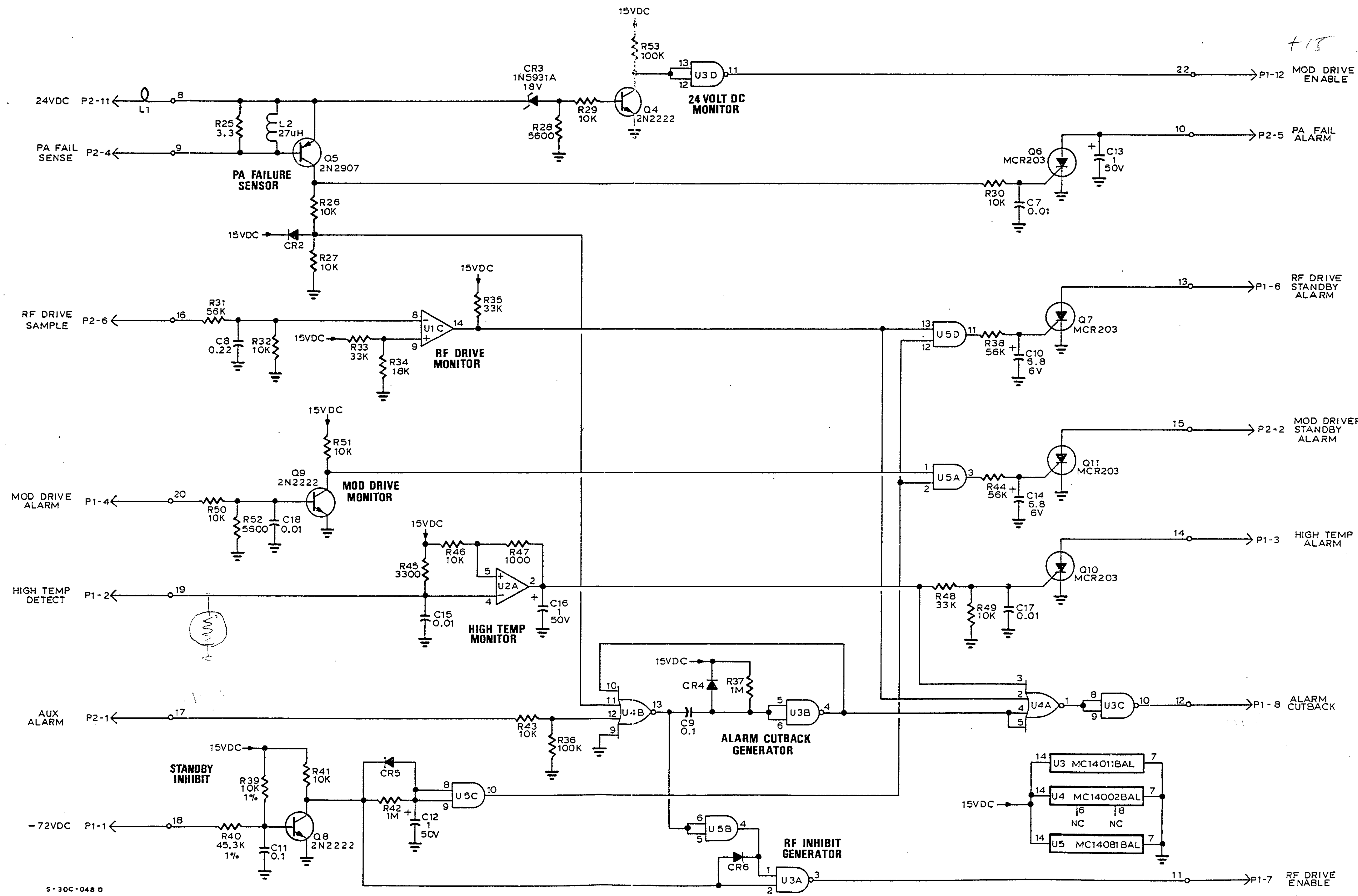

Figure FO-3 Electrical Schematic - NAPC7 Monitor Module (Sheet 2 of 2)

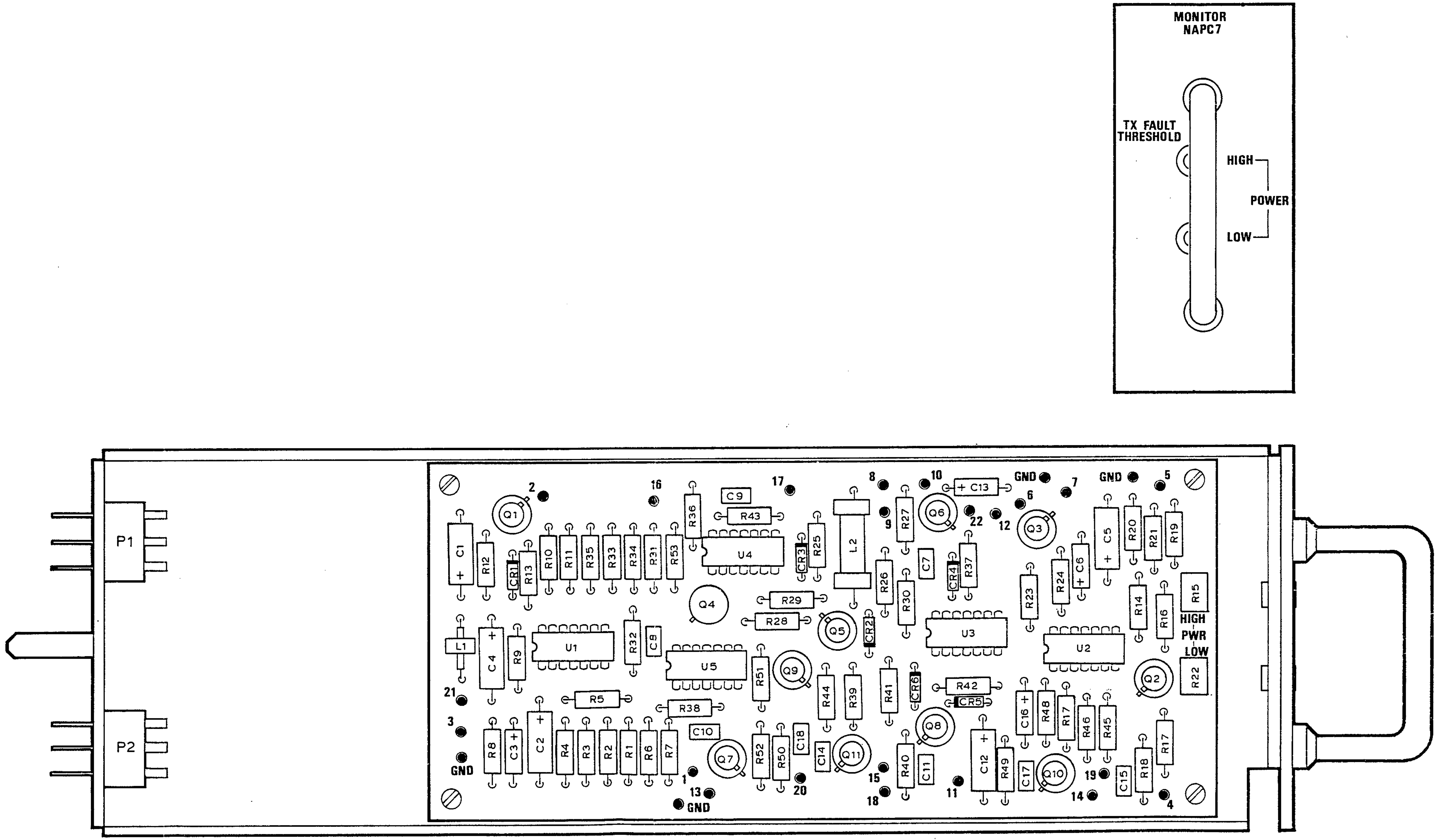

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Figure FO-4 Assembly Detail - NAPC7 Monitor Module